









NAVAL POSTGRADUATE SCHOOL Monterey, California



THESIS

EMULATION OF THE AN/UYK-20 TACTICAL DATA COMPUTER ON THE BURROUGHS D-MACHINE

by

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March 1977

Thesis Advisor:

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Emulation
of the
AN/UYK-20
Tactical Data Computer
on the
Burroughs D-machine

bУ

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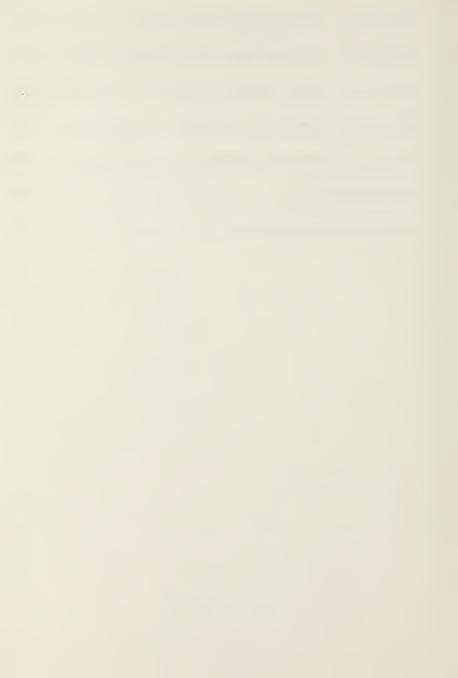
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I. INTRODUCTION

A. STATEMENT OF THE PROBLEM

The Navy has been challenged with maintaining the newest, most efficient tactical data systems consistent with the continually increasing demands and requirements of the real-time environment. There is an extensive conversion effort required to change from existing systems to newer more sophisticated technology such as the AN/UYK-20. Inherent in upgrading to a new system is the complex software redesign and modification process which is often hindered by the absence of the new computer system.

Unfortunately, the demands of a military installation require software generation prior to implementation of an upgraded computer system. One solution to this problem is to utilize for software development an intermediate computer system which has the capability of emulating the anticipated target machine. This provides a vehicle for software design, development, and testing prior to transitioning to the new system.

Currently, the Naval Postgraduate School (NPS) Computer Science Department maintains a Burroughs Interpreter-Based System known as the Burroughs D-machine. The D-machine is capable of being microprogrammed to emulate any of a miriad



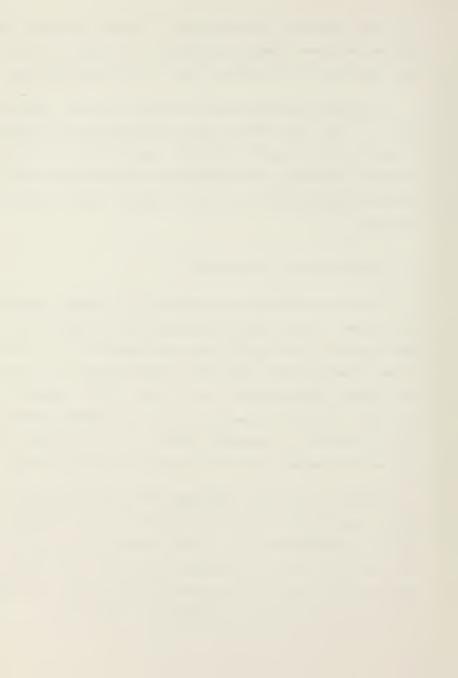
of target machines. It effectively enables students to create their own computer knowing only the machine instruction repertoire for the control unit in the target machine.

The problem presented was to develop a feasible working model of the AN/UYK-20 on the microprogrammable Burroughs D-machine. The project provided an opportunity- to obtain practical experience with contemporary hardware and to manipulate writeable control stores to imitate a Navy tactical computer.

B. APPLICATIONS OF THE AN/UYK-20

The Univac AN/UYK-20 minicomputer is a general purpose militarized digital computer adaptable to numerous tactical applications. The AN/UYK-20 has been successfully utilized in many time-critical, real-time systems including fire control radar, communication controllers, signal processing analyzers for sonar and beacon signals, and numerous weapons control systems. A subsequent chapter will be devoted to the technical aspects and internal design of the AN/UYK-20.

Because of its size, ruggedness, and computing capabilities, the AN/UYK-20 has been designated the Navy's standard tactical minicomputer [16]. It was selected for emulation in order to provide a feasible platform for software development to those military installations either contemplating or in the process of receiving an AN/UYK-20.



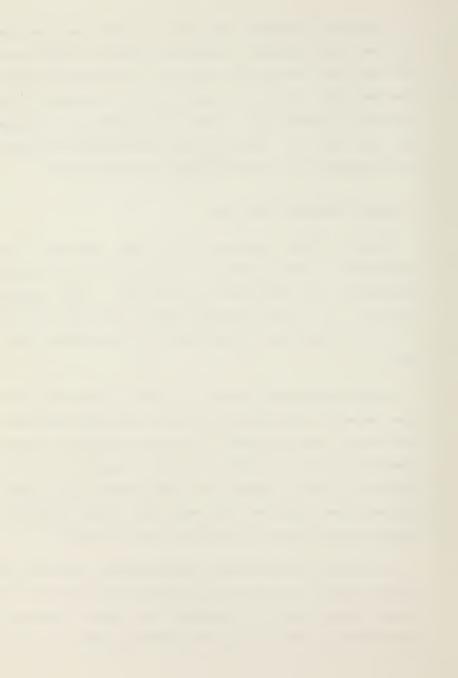
A workable emulation would allow military applications such as data reduction, navigation, telemetry, sensor processing, range tracking and logistics to have software packages developed, tested, and modified prior to arrival of the AN/UYK-20. Furthermore, it would permit personnel to become familiar with the machine by providing advanced training, thereby easing the transition phase to the new system.

C. PROJECT DESIGN OBJECTIVES

Several design techniques were used throughout the development of this project: 1) modularity, 2) structured programming, and 3) extensive documentation. These design features will aid the interested reader as well as simplify any future extensions or modifications to the existing emulation.

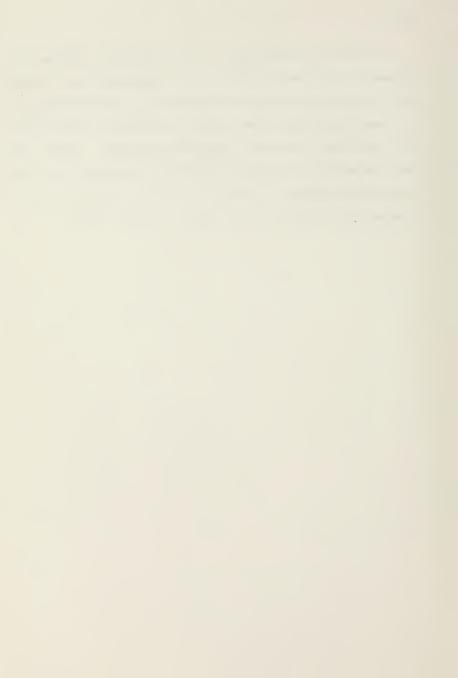
Modular design was utilized by creating independent program segments which were individually developed, debugged, and tested. These modules or subroutines provided a strong foundation which were readily modified throughout the entire programming effort. Conceptually, the emulation was divided into relatively small entities which were further reduced to program segments rarely exceeding one page in length.

Structured programming was demonstrated by utilizing a limited number of control flow structures and maintaining a common logical design throughout the entire emulation. Comprehensible code held precedence over extremely efficient



code.

In addition to modularity and structured programming, the entire programming endeavor was supplemented with extensive commenting to provide the necessary self-documentation to promote and facilitate program translation, modification, and fusing with the other independent modules. These concepts promoted the extensive team effort required to achieve the research goals. In addition, it will provide ease of program maintenance and modification in the future.



II. EMULATION

A. HISTORICAL BACKGROUND

The term microprogramming was first utilized in an article by Professor M. V. Wilkes of the Cambridge University Mathematical Laboratory in 1951 [24]. His paper concentrated on a control section within the computer which, when programmatically controlled, performed register-to-register data transfers sequentially and in parallel for the execution of a single machine instruction. A sequence of operations (microinstructions) required for execution of a machine instruction is considered a microprogram.

Traditionally, the computer has been composed of essentially five components: the arithmetic/logic unit, the control unit, memory or storage, input, and output (Figure II-1). The control section sets the proper conditions for the opening and closing of required gates in the logic network. Historically, the control section has been hardware consisting of a series of decoders and flip-flops along with their associated circuitry. Therefore, every machine instruction had a fixed interpretation which was hardwired within the control unit.

In 1957, Wilke's definition of microprogramming was slightly modified. It was defined as a technique of design-



ing the control circuits of an electronic digital computer to interpret and execute a given set of machine operations as an equivalent set of micro-operations [15].

The hardwired control section can be modified by interchanging ROM modules or other hardware components, by replacing the control section with a programmable (dynamically writeable) control store which in itself is a separate word-organized memory (Figure II-2) or by combining both approaches. A programmable control store allows rapid changes in the machine's instruction repertoire while maintaining maximum design flexibility. The resulting computer system is microprogrammable and capable of storing a series of changeable machine personalities.

The computer control store can thus be modified to allow the execution of machine language programs intended for a variety of machine architectures. This process can be compared to replacing hardware components found in conventionally designed computer systems. The primary advantage of microprogrammed logic is the capability to perform various control sequences without hardware modifications. The process through which the hardware components of one machine (host) are made to imitate the specific hardware characteristics of another machine (target) is known as emulation.



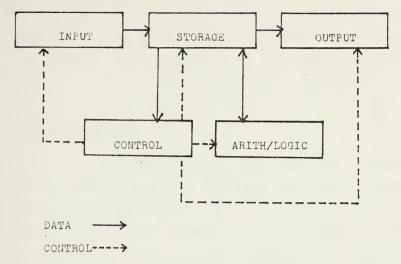


Figure II-1 [11]

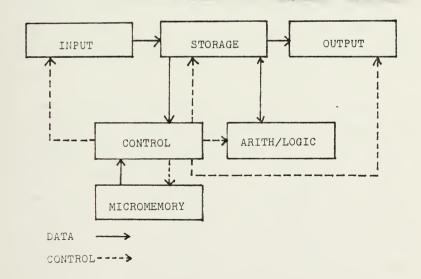


Figure II-2



Emulation allows the computer scientist to create various machine architectures from a single microprogrammable
host. The complete set of microprograms (firmware) and the
necessary hardware, as well as the required software, added
to one computer system enabling it to execute programs
designed for another system is known as an emulator.

B. MICROPROGRAMMING

Computer manufacturers have made available numerous microprogrammable machines which permit the user to tailor his instruction repertoire to meet the needs of his particular application. Some examples of microprogrammable computer systems are the Burroughs D-machine, the Nanodata QM-1, the Varian 73, the Standard Logic CASH-8, or the Hewlett-Packard 2100. These microprogrammable systems provide the benefits of flexibility, lower system costs and a systematic approach to system design if utilized effectively.

When a manufacturer designs a dynamically writeable control store, the amount of parallelism to be allowed must be determined. Parallelism is defined to be the simultaneous control of numerous hardware resources. There are basically three forms of control: vertical, horizontal, and residual. In vertical microprogrammina, each instruction controls a single operation with program flow being sequential, unless the instruction was a conditional or unconditional branch. By contrast, a horizontally microprogrammed machine is



programmed via instructions which simultaneously control multiple resources including condition testing and microinstruction sequencing.

Horizontal microinstructions usually are not encoded which means each bit controls one machine resource or operation. They usually have a wider word than vertical instructions and consequently consume more memory. Vertical instructions are usually encoded with one or two levels. Encoding means the value of a control field in the microinstruction is a binary code specifying which resource or operation is to be performed. The horizontal microinstructions have the potential of being much more efficient resource managers and consequently are more difficult to optimally design than their vertical counterparts.

Combining the attributes of horizontal and vertical microprogramming results in residual control. This method saves memory by using vertical microinstructions while simultaneously controlling multiple parallel resources via setup registers.

Microinstruction implementation severely effects the speed of microprogram execution. In serial implementation, one microinstruction is fetched and fully executed prior to fetching the next instruction. This technique offers the advantage of logical simplicity while suffering from lack of efficiency since it consumes the maximum amount of time.

'Parallel' implementation permits fetching of the next



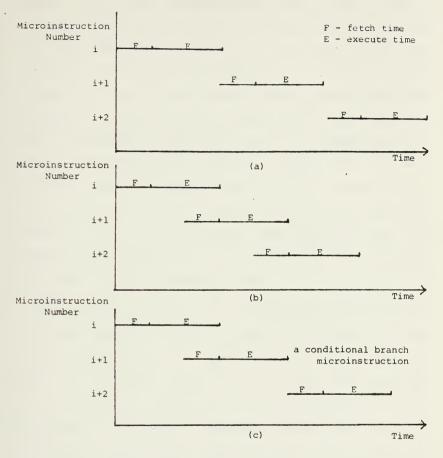
instruction before termination of the previous instruction.

The obvious advantage is execution speed which is of utmost importance when emulating another machine (Figure II-3) [2].

Another significant microprogramming characteristic is the number of phases used in the execution of each microinstruction. A monophase system means there are no subdivisions of the basic clock pulse and consequently each microinstruction is controlled by the transmission of the leading edge of a clock cycle. In a polyphase implementation scheme, the basic clock cycle is subdivided into minor phases which are independently generated via hardware. Although polyphase operations are more complex and require complicated control, they do permit faster resource manipulation when they are efficiently coded by allowing multiple operations to be performed during the same phase(s).

The microprogrammability of a given computer and the capabilities of its associated microprogramming language are directly effected by the the presence or absence of each of the alternative microprogramming characteristics described above. The microprogramming language spectrum ranges from the lowest level or microlanguage through the assembly languages to the high level procedural languages.





(a) Serial fetch and execute.

- (b) Parallel fetch and execute.
- (c) Combined serial-parallel where next address depends on conditions in present cycle.

Figure II-3 [2]



The problems of microprogramming can be significantly reduced if suitable software support exists and is readily available. This support is usually in the form of simulators and debuggers. Typically, a simulator provides an alternative to assembly level coding by permitting the user to code in a higher level language and yet achieve the same results at the expense of some added memory and execution time. Debuggers are extremely useful in the developmental stages of microprogramming especially for new and experimental system design. Debuggers permit dynamic access to the machine status and register contents at the instant they are employed, i.e. a trace feature. Some debuggers offer the opportunity of assembling in-line. This option can drastically reduce required debugging time.

The primary application of microprogramming is to implement the necessary control structure required for the analysis and execution of machine level instructions by means of programmed control stores rather than hardwired logic. Therefore, a dynamically microprogrammable computer can provide a software development system which can be a cost-effective approach to experimentation with potential candidates for replacement computer systems or the design of completely new systems to fit the needs of unique applications.



C. THE GOALS OF EMULATION

A well-designed emulation can provide an opportunity to experiment and create software for new computer systems before the actual hardware is available. The utilization of an emulator can almost eliminate reprogramming, consequently smoothing the system transition period. In addition, emulation has provided a workable model of new systems under consideration for procurement, providing a much more detailed cost-benefit analysis of system conversion.

Furthermore, it is often economically sound to emulate a second generation computer with a third generation system. This provides growth to a contemporary system while fulfilling the requirements of the past in a cost-effective manner. However, this can be a disadvantage if the programming staff uses the emulation as a link to the old system and consequently fails to take advantage of the attributes of the new system.

D. EMULATION VERSUS SIMULATION

To accomplish the emulation objectives, certain design features must be incorporated into an emulation. Naturally, execution time and allocated memory are the two foremost considerations. Traditionally, the concept of mimicking another computer has been accomplished by either a simulator or an emulator, two concepts often confused with one another.



A simulator is a series of high level language (HLL) or assembly language statements which individually do not behave like the target machine instructions. The host machine executes its own native instructions in order to imitate the target machine operations. Consequently, simulation is a rather slow technique because it requires an intermediate translation. In addition, simulation of certain instructions such as bit manipulation and shifting operations can require an enormous amount of intermediate code generation demanding a significantly larger memory allocation.

An emulator is a microprogram that is executed on the host machine, performing machine instructions of the target machine. Since an emulator accepts the binary object code of the target machine and directly executes these instructions, it can be extremely efficient in terms of time and space requirements. The execution time of an emulation is dependent upon many factors: clock rates of the two machines, frequency of memory references, high speed shifting compatibility, required register mapping between target and host machines, bit manipulation capability of the two machines, condition code selection and testing, flexible data path selection capability, interrupt similaritites, input/output compatibility, and microprogramming efficiency. If the hardware features between target and host machines are extremely compatible and highly efficient microprogramming has been employed, an emulation performance ratio (host



to target) of nearly one to one can be attained. This emulation performance ratio (EPR) has been demonstrated by the emulation of the SKC-2070 on the Nanodata GM-1 computer. It is possible to achieve an EPR better than one to one under ideal situations, when the host machine has a much faster internal operation execution rate [1].

Several distinct advantages can be realized using emulation as compared to simulation. The execution speed is significantly better by at least an order of magnitude. The target machine representation in firmware is closer to the actual hardware design and total access to the lowest machine level is achievable. Perhaps most noteworthy, emulation provides the opportunity to rapidly create test beds for numerous machine architectures and provide a basis for new system development.

E. EMULATION TECHNIQUES

Iraditionally, there have been three approaches for emulating machine instructions: 1) hardware or firmware assistance to a software simulation as demonstrated by the IBM 360/o5 emulation of the IBM 7090, 2) independent host system hardware or firmware which provides for complete execution of the target machine's instruction repertoire of which the Burroughs D-machine emulation of the AN/UYK-20 is an example, and 3) an auxiliary processor which is operated in conjunction with the host machine to execute target machine instructions [14].



Software-controlled emulation is usually characterized by categorizing the target machine instructions into three distinct classes: easily emulated instructions, complex instructions not readily emulated, and those instructions not deemed necessary for the desired application. Instruction usage is significant in this classification process. Each class of instructions becomes a candidate for direct hardware or firmware implementation. The first emulated function in this approach is usually the fetch and analysis operation. After the instruction is analyzed, the appropriate opcode subfunction can be executed.

An alternative emulation technique is the firmware—controlled method. This approach is identified by having system control reside completely in firmware or hardware during the emulation process. All instructions are executed on the host machine as if they were indigenous to the target machine. This method is much more efficient than the software—controlled technique; however, it is more expensive and the cost differential is directly related to the required performance level. Performance is dependent upon the number of required data paths, arithmetic units, and other additional logic circuitry which must supplement the host machine architecture.

Upon entering the emulation mode in a firmware-controlled emulator, the machine performs like the target machine until encountering an exit situation. There exists three exit modes: 1) priority interrupt, 2) not implemented



instruction, and 3) deliberate exit because of a debugging routine.

The third emulation technique consists of utilizing auxiliary hardware electronically attached to the host computer for the sole purpose of executing target machine instructions. In effect, a target machine is composed of host machine hardware with the necessary additional components required to create an effective emulator.

F. EMULATION HARDWARE

The development of writeable control stores and microprogramming techniques have significantly influenced computer design. This section will describe some of the available dynamically microprogrammable hardware (Figure II-4).

The Hewlett-Packard 2100 is a general purpose minicomputer. It has a unique control store divided into two segments. One section is ROM and the other section is user programmable. The machine is vertically microprogrammed using a standard 80 instruction machine language repertoire. A debugger and assembler assist the user in microprogram development [2].

The Standard Logic CASH-8 is a high speed digital controller with a separate control store. It consists of 16 general purpose registers and an accumulator. The CASH-8 is vertically microprogrammed but does not support any language



above microlanguage [2].

The Varian 73 is a general purpose minicomputer that has a 150 instruction set. The horizontal microinstruction consists of 64 bits with 25 fields, some of which indicate register transfers, ALU operations, shifting, control store addressing, condition testing, I/O control and memory operations. The Varian 73 contains both a ROM control store and a writeable control store loadable from main memory. A microprogram assembler and interactive simulator are available [2].

The Nanodata QM-1 is unique in that it contains both a control store and a nanostore which are both loaded under user program control. The 18-bit vertical microinstructions are stored in the control store, fetched and then interpreted under nanoprogram control. A horizontal nanoinstruction is 360 bits which is subdivided into five 72-bit vectors. Assemblers for both microprograms and nanoprograms are available [2].

The previously described machines represent a small sample of the available microprogrammable computer architectures. The availability and flexibility of these computer systems has stimulated demand for these devices. Consequently, hardware manufacturers have been compelled to produce writeable control store equipment to satiate the needs of the computer market.



CONTROL STORE REALIZATION		USER MICROPROGRAMMABLE
Main Memory	• IBM S/360 Model 25 IBM S/370	• Burroughs B1700 • Nanodata QM-1
	Interda	ata 85 •
		Varian 73
Fast Read/ Fast Write	Hewlett Packard 2100	
		DSC Meta 4
ROM	• Interdata 80 IBM S/360 Models 30, RCA Spectra 70 Model	
	None Preparatio User Micropr	n of Provision of ograms Translator or Simulator

SUPPORT AVAILABLE TO USERS

Note: Relative microprogrammability is the distance from the origin to the machine point in two space.

Figure II-4 [2]



III. AN/UYK-20 ARCHITECTURE

Constructing an efficient emulation requires a precise understanding of the architecture and performance characteristics of the machine being emulated. An emulation must attempt to match the target machine's features and maintain its flexibility of hardware design as closely as possible. Although it is not required, an operational demonstration of the emulated machine can solve many emulation questions.

In emulating the AN/UYK-20, architecture and performance criteria were derived from technical publications, since an actual machine was unavailable. When inconsistenties appeared in the documentation, specific questions were posed to a UNIVAC field engineer, who often tested programs on the AN/UYK-20 to resolve inconsistencies. Documentation coupled with an expert consultant provided sufficient information for emulating the AN/UYK-20 successfully.

The intent of this chapter is to outline those features of the AN/UYK-20 significant to the emulation. A detailed hardware description can be found in Refs. 20, 22, 28.



A. HARDWARE DESIGN

The AN/UYK-20 was designed for the Navy to fulfill the requirements for small or medium size general purpose data processing in shipboard, mobile shelter, or other military environments. Sperry Univac incorporated minicomputer technology in constructing the AN/UYK-20, including MSI circuitry design, microprogrammed control, memory modularity, and asynchronous or synchronous input/output channels.

The AN/UYK-20 had to be extremely flexible in its applications, offering a wide range of configuration possibilities which were derivatives of the basic design. Modularity, a concept highly desirable in a military environment, was achieved by offering options that could be easily addedusing printed circuit cards and/or memory modules.

The AN/UYK-20 can accommodate up to eight 8K, sixteen-bit word boards of magnetic core storage with an access time of 750 nanoseconds. The central processor is controlled by a programmable micromemory which can be expanded by an additional 512 words. The microprogram controller is programmed at the factory, but the additional micromemory option is user defined. Both sections of micromemory are programmed using fusible links, and once programmed they are completely static (Figure III-1).

A memory interface is responsible for the transfer of data to memory from the central processor (CP) and input/output controller (IOC). Both the IOC and the CP are



capable of accessing all of memory (65,536 words maximum). The addition of direct memory access (DMA) provides a second memory interface and an additional access port which is connected to each of the two 32K memory segments.

The input/output controller permits the central processor to communicate with the external devices without interfering with program execution. The IOC has a maximum of 16 parallel or serial channels. Parallel data transfer takes place asynchronously using 8-bit, 16-bit, or 32-bit transfers. Serial interfaces are either synchronous or asynchronous, with word-to-serial or serial-to-word conversions occurring in the IOC. The IOC and CP compete for memory access through the memory interface with priority given to the IOC in the event of a simultaneous request. The IOC is permanently assigned several memory addresses for command word and interrupt word storage.

The addressable high-speed registers available in the AN/UYK-20 include the program address register (P-register), two 16-bit status registers (SR1 and SR2), a real-time clock register (32-bits), a monitor clock register (16-bits), and a set of sixteen 16-bit general registers. An additional stack of 16 general registers is an available hardware option.

The sixteen general registers were included to enhance the speed and performance of the AN/UYK-20, allowing most programs to use a great proportion of register-to-register



instructions. These general registers can be used as accumulators for arithmetic, shift, or logical functions, as index registers, or as temporary storage locations. The second set of general registers can be readily employed via a status bit. This status bit designates which general register stack is to be utilized. The duplicate set of general registers yields dividends in a multi-task or heavy-interrupt processing environment. This additional register set can be used to provide high-speed temporary storage, thus avoiding slower main memory storage of working variables.

The two 16-bit status registers and the program address register represent the machine status of the AN/UYK-20. When these registers are collectively referenced, they are called the program status word (48-bit PSW). The P-register indicates the next instruction to be executed. This instruction may be a 16-bit single-word instruction or a 32-bit double-word instruction. Program control can be modified by using an instruction which manipulates the contents of the P-register.

Status register 1 contains bit information concerning condition code settings, overflow, and carry bits, interrupt codes, and numerous other machine indications (Figure III-2).



AN/UYK-20 FUNCTIONAL ARCHITECTURE

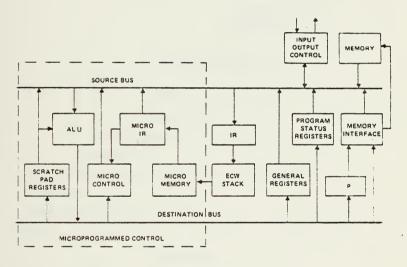
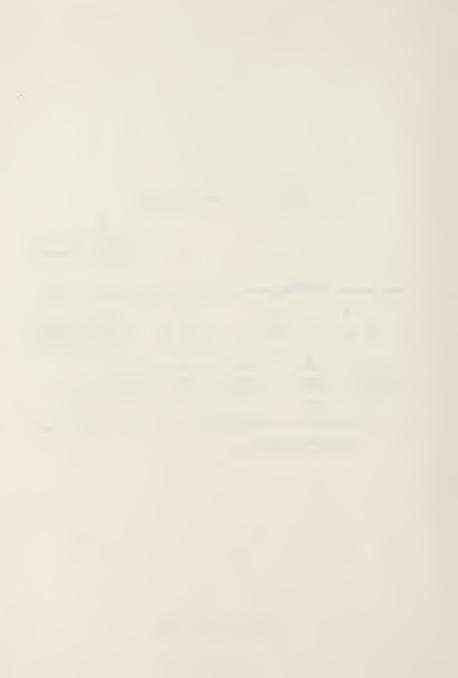


Figure III-1 [22]



STATUS REGISTER 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
															1 -	NABLE (1) OR DISABLE
																(1) OR LOCKOUT (0)
																OR LOCKOUT (0)
													SSI			CKOUT (0) UPTS
									EN	NO.	USE		POL	NT R	OLIN	(D)
									OR	PROV	IDE	RESIG	OUE (1)	_	
										(0) (0) U-WO.						ERISTIC S
							со	NOIT	ON C	00E 0	ESIG	NAT) R			
									NATO	R						
			NO				MEM		(1) RE	FERE	NCE	FOR	ADDE	RESS	00-7	7, 300-477
		NOT	r USE		31, 11			J	,			J.1				., ,
	GEN	ERA	LREC	ISTE	R SET	0 (0	OR:	SET 1	(1) A	CTIVE						
NOT	USE	0														

CONDITION CODES

SR BITS 8 and 9	ARITHMETIC	COMPARE
00	0	$(R_a) = (R_m)$ or (Y)
01	>0 (POS)	$(R_a) > (R_m) \text{ or } (Y)$
10	Not Used	Not Used
11	<0 (NEG)	$(R_a) < (R_m) \text{ or } (Y)$

Figure III-2 [23]



Status register 2 holds control bits for direct or indirect addressing, and holds interrupt codes. Interrupt processing routines set bits in the interrupt code field corresponding to the IOC interrupt (Figure III-3).

STATUS REGISTER 2

		12	11	10	9	8	7	6	5	4	3	2		0
				INTERRUPT CODE										
	İ		IND	INDIRECT CONTROL BITS FOR R12										
INDIRECT CONTROL BITS FOR R14														

INDIRECT CONTROL BITS	MEANING
00	Normal Addressing.
01	Normal Addressing.
10	Indirect Addressing w/o indexing;
	IWl at $Y = y$.
11	Indirect Addressing with indexing;
	IW1 at Y = y + (Rm).

Figure III-3 [23]

The real-time clock and monitor clock registers provide program-controlled interrupt capability which is useful for timing and synchronizing program segments with real-time events. The real-time clock (RTC) is a 32-bit register used as count-up storage while the monitor clock (MON) is a 16-bit count-down register. A one kHz internal oscillator controls the counting speed of both registers. An optional



external clock operating at a frequency up to 50 kHz is also available.

Interrupt processing in the AN/UYK-20 is conducted using a priority level scheme which classifies interrupts into three priority levels (classes). Interrupts within the same class are assigned a priority ranking and a code which identifies which processing routine to execute. During interrupt handling, all interrupts of the same level or lower level are locked out until the CP is completed processing the current interrupt. Higher priority interrupts can override the lockout and cause the CP to honor them first, holding the lower level interrupts in abeyance until higher level interrupt processing is completed. The highest priority interrupts are hardware malfunctions, followed by software interrupts, and at the lowest level, IOC interrupts.

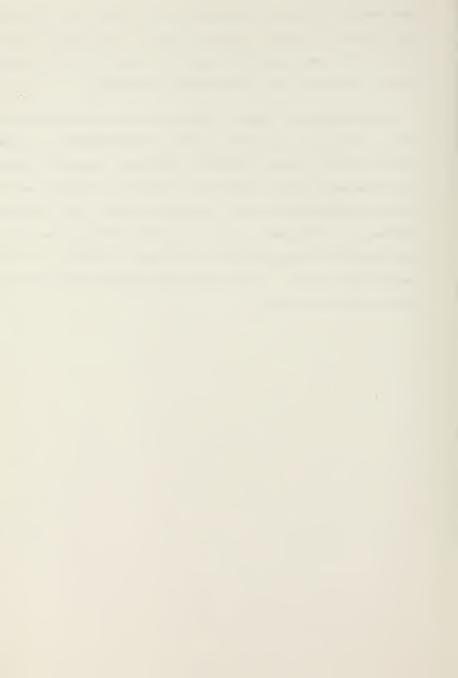
Permanent locations in memory corresponding to each interrupt class hold the PSW and RTC when an interrupt is being honored. Likewise, other permanent memory addresses assigned to each interrupt class hold the appropriate interrupt routine entrance location to be loaded into the PSW.

Memory addressing is accomplished using 64 page address registers which separate memory into 1024-word pages. Absolute addresses are formed by isolating the upper six bits of the relative address to find the page address register number, and then concatenating the lower six bits of the



page address register contents with the lower ten bits of the relative address (Figure III-4). Any operation that stores into memory sets the most significant bit of the page address register used in generating the address.

Some additional hardware features of the AN/UYK-20 are those functions available on the maintenance panel of the machine itself. These include a breakpoint feature which allows an operator to insert from the panel an address which causes the AN/UYK-20 to stop execution when the selected address is referenced. Other available toggles allow halting execution programmatically using Key 1 or Key 2 on the maintenance panel. These additional hardware features are useful debugging tools.



MEMORY ADDRESS GENERATION

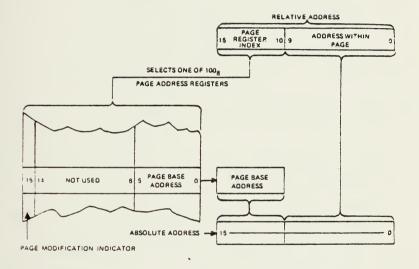


Figure III-4 [22]

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B. INSTRUCTION FORMATS AND REPERTOIRE

1. Repertoire of Instructions

The AN/UYK-20 instruction set is composed of nearly 260 separate instructions designed to be both versatile and comprehensive. Both single-word (16-bit) and double-word (32-bit) instructions are available. Some of these instructions are specifically designed to meet the requirements of a real-time environment. A few sample instructions include:

- a. Local jumo used to facilitate loops, saving several steps in program execution.
- b. Reverse register used in a communication environment when data is received in one sequence but must be transmitted in reverse sequence.
- c. Set bit, clear bit, and test bit used to test individual bits in registers saving considerable execution time in programs that communicate via flags and status words.

Additional flexibility is provided when the 'math pac' hardware option is included in the AN/UYK-20 configuration. Some 33 additional opcodes are added to the instruction set in order to increase the computational capabilities of the machine. An instruction for square root, double precision multiply/divide instructions, as well as hardware trigonometric and hyperbolic functions which utilize coordinate conversion algorithms (cordic) are included.



Single-word instructions are generally employed when manipulating operands in high-speed registers. Double-word instructions are used in operations involving direct or indirect addressing with or without indexing, or supplying 16-bit constants to programs. Typical instruction speeds for a single-word versus a double-word instruction are:

	SINGLE-WORD	DOUBLE-WORD
ADD	.75 - 1.5 usec	1.5 - 2.25 usec
LOAD	.75 - 1.5 usec	1.5 - 2.25 usec
MULTIPLY	3.8 - 4.0 usec '	4.4 - 4.6 usec
DIVIDE	6.8 - 7.0 usec	7.4 - 7.5 usec

Nearly all instructions affect condition bits in status register 1. The AN/UYK-20 sets these bits as a result of two types of operations. Most instructions that do not involve compare logic are categorized as arithmetic instructions. When the result of the arithmetic operation is determined and is about to be stored in memory or a register, a condition code is set indicating whether the result is positive, negative, or zero. Compare instructions set the condition bits based on a greater than, less than, or equal to comparison of two registers or a register and the contents of a memory address.

Two other bits in SR1 are set as a result of computational or shifting instructions. The overflow designator is set whenever an arithmetic or shift operation requires more bits than are provided for in a register (16 bits).



The carry designator is set when an arithmetic operator generates a carry beyond the most significant bit of the register.

The AN/UYK-20 allows five different types of operand formats: single-length, byte, literal, optional floating point, and double-length. Single-length operands are 16-bit values with the sign bit assumed to be in the most significant bit. In arithmetic calculations, the single-length word is assumed to be a two's complement integer. Byte operands are considered 8-bit unsigned integers, and can be the most significant or least significant half-word of a memory location. Literal operands are 4-bit unsigned integers denoted by the 'm' field of a literal type instruction. Floating point operands are formed using two adjacent registers or memory locations with fields containing the sign of the fraction, the characteristic, and 24 bits of the fraction.

Double-length operands are concatenated from two adjacent registers or two adjacent memory addresses. The most significant half of the double-length operand is contained in the low-order register or memory address, and the least significant half in the next sequential register or address. The sign bit for both words resides in the high-order bit position of the most significant half-word and when used in an arithmetic calculation, the double-length operand is treated as a two's complement integer. Instructions involving double-length operands require the low-order



register or memory address to be even, since the adjacent cell address is formed by 'OR'-ing a 1 in the least significant bit of the address.

2. Instruction Format

The AN/UYK-20 has five different instruction word formats, designated by two-letter mnemonic codes. These codes are: RR (Register-Register), RL (Register-Literal), RI (Register-Immediate), RK (Register-Constant), and RX (Register-Index). Each of these formats are designated in the instruction word by a combination of the opcode field and the subfunction code. Registers are identified in the 'a' and 'm' fields of the instruction, and are referred to by the notation Ra and Rm. The 'v' field is treated as an address or arithmetic constant, depending on the instruction (Figure III-5).

The format RR single-word instructions perform operations involving the registers specified by the 'a' and 'm' fields. No memory references are made to access operands, causing considerable savings in execution time. The 'a' or 'm' field may be used to index special operations on registers.

Format RL instructions use a 16-bit instruction word, using one or two general registers. The 'a' designator selects the general register Ra or register pair Ra, Ra + 1. The 'm' designator contains the 4-bit literal value which will be used in the instruction.



INSTRUCTIO	N FORMATS								
	15 14 13 12 11 10	9 8	7 6 5 4	3 2 1 0					
RR	Op*	υ	a	m					
	a selects R _a ; m s	elects	R _m .						
	15 14 13 12 11 10	9 8	7 6 5 4	3 2 1 0					
RL	Op*	0	a	m					
	a selects R _a ; m c	ontai	ns 4-bit cor	nstants.					
RI-1	15 14 13 12 11 10	9 8	7 6 5 4	3 2 1 0					
Local Jump	Op*	1		d					
	d is signed numb (+ is forward; —	er of	instruction (kward)	ns to jump,	relative to current position.				
	15 14 13 12 11 10	9 8	7 6 5 4	3 2 1 0					
RI-2 Indexed Memory	Op°	1	a	m					
,	a selects R_a , m selects R_m . R_m selects memory address.								
	15 14 13 12 11 10	9 8	7 6 5 4	3 2 1 0	15 14 13 12 11 10 9 8 7 6 5 4 3 2 10				
RK	Op*	2	a	m	У				
	a selects R _a ; m ≠ Operand = y + R			n = 0 selects	5 0.				
	15 14 13 12 11 10	9 8	7 6 5 4	3 2 1 0	15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0				
RX	Op*	3	• a	m	ν .				
	a selects R _a , m ≠				i O.				
	v + R or 0 sele	CIO III	emury addi	C22.					

Figure III-5 [23]

^{*}Op is operation code



R1 format single-word instructions are separated into two catagories. RI Type 1 instructions are local jump instructions where the P-register is increased or decreased by the 'd' field in the instruction. The 'd' field represents the two's complement deviation value and allows the P-register to be altered a maximum of +177 octal or -200 octal. RI Type 2 instructions involve operations that use the general registers Ra and Rm, and a memory address specified by the contents of Rm.

The format RK instructions contain 32 bits of information. The upper 16-bits contain the operation code and the designator fields. The 'a' field selects the general register Ra, and the 'm' field denotes how the next word, containing 'y', is to be used. If 'm' equals zero, then the effective operand address Y, equals 'y'. If 'm' does not equal zero, then Y is formed by adding the contents of Rm to 'y'.

Format RX are double-word instructions similar to the RK instruction that use direct and indirect addressing techniques determined by the 'm' field. If the 'm' field equals zero, then direct addressing without indexing is employed, with the effective operand address formed from the 'y' field itself. If the 'm' field equals 1 through 7, 11, 13, 15, or 17 (octal), then direct addressing with indexing is employed. The effective operand address is formed by adding the contents of Rm to 'y'. An 'm' field value of 10, 12, 14, or 16 (octal) indicates indirection is to be



employed, and the indirect address control fields in status register 2 contain information which is used to generate the effective operand address or a pair of indirect words. When the control fields equal 0 or 1, then direct addressing with indexing results. If the control field equals 2, then the contents of the first indirect word (IW1) is located at 'y'. Finally, if the control field equals 3, then IW1 is located at 'y' indexed by the contents of Rm. Indirect word format is shown in Figure III-6. Cascaded indirection is possible provided that the indirect words are properly encoded.

Byte addressing is accomplished using RX format instructions. A byte identifier (B) is used to determine which half-word (8-bit) is to be referenced. If B equals 0, then the most significant half-word in address Y is the operand byte. If B equals 1, then the least significant byte at Y is the operand. The least significant bit in the indexing register is used as the byte identifier, and the remaining 15 bits are used as the indexing value for finding Y. Indirect byte operand addressing formulae are included in Figure III-o. The following formulae apply for direct byte operand addressing:

m=0, Y=y, and B=0 m=1-7, 11, 13, 15, or 17 octal Y=y + (Rm)/2 and B=LSB of (Rm)



The preceding section has described the fundamentals of the AN/UYK-20 instruction formats. References 21 and 23 should be consulted for further information concerning instruction formats and decoding.

INDIRECT WORD FORMATS

15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

NOT	1	J	NOT USED	×	IW 1
			IW 2		IW 2

OCTAL J VALUE	ADDRESS DETERMINATION
0	Y = 1W2; if byte mode, upper byte is used.
1	Y = IW2 + (Rx); if byte mode, LS8 of Rx determines byte. *
2	Y = IW2 + (Rm); if byte made, LSB of Rm determines byte. *
3	Y = IW2 + (Rm+1); if byte mode, LSB of Rm+1 determines byte. *

^{1 = 0.} DIRECT ADDRESSING, OPERAND AT ADDRESS Y

Figure III-6 [23]

^{1 = 1,} CASCADED INDIRECT ADDRESSING, NEW INDIRECT WORD 1 AT ADDRESS Y

^{*} To determine the operand address when in byte mode, the contents of R_x , or R_m , or R_{m+1} are right shifted 1 bit position and zero filled in the left most position



IV. BURROUGHS D-MACHINE

A. HARDWARE DESCRIPTION

The microprogramming facility at the Naval Postgraduate School is composed of a Burroughs Interpreter-Based system. This system possesses the characteristic of being dynamically microprogrammable and is designed using a simple building block structure. A typical system is made up of a number of interpreters (processors), main memory modules, and input/output devices, along with a switch interlock device (SWI) controlling data flow on the data bus connecting the interpreters to main memory and peripheral devices. The heart of the system is the interpreter, also referred to as the D-machine.

A D-machine possesses five functional modules: the logic unit (LU), the control unit (CU), the memory unit (MU), nanomemory (NM), and microprogram memory (MPM). The system presently installed in the Computer Science Department combines nanomemory and microprogram memory into one functional unit. The architecture of the D-machine is designed around 8-bit word slices. Word lengths from 8 bits to 64 bits are permissible using the same functional unit (Figure IV-1).



INTERPRETER BLOCK DIAGRAM

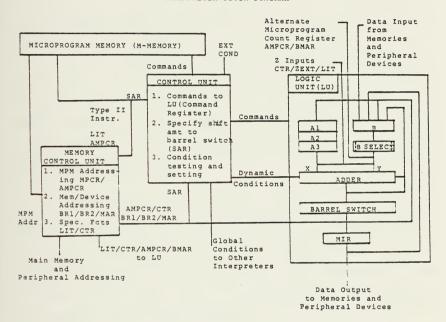


Figure IV-1 [o]



The D-machine used for this thesis has been configured as a 32-bit word processor. Reference 17 provides a thorough and concise description of the architecture of an interpreter-based microprogramming system. Reference 6 details the specifics of D-machine microprogramming which must be thoroughly understood by the programmer.

1. Logic Unit

The D-machine's logic unit performs shifting, arithmetic, and logic functions and contains scratch pad registers and data interfaces for the switch interlock. All adder operations are performed using two's complement arithmetic, and shifting is accomplished in a matrix of gates called the barrel switch.

The scratch pad registers A1, A2, and A3 are identical in function. They act as temporary storage registers
within the D-machine and serve as primary inputs to the
adder. The control unit determines which register will be
an input to the adder. Any of the A-registers can receive
the output from the barrel switch.

The B register functions as the primary external input interface from the switch interlock. It acts as the second input to the adder and can receive certain direct inputs from the adder's arithmetic operations. The B register can be loaded from any of the following sources:



- a. The barrel switch output.
- b. The adder output.
- c. External data from the switch interlock (or control panel switches).
- d. The memory information register (MIR).
- e. The complements of four bit or eight bit carries.
- f. The barrel switch ORed with the adder, external data from the switch interlock, or MIR.

The output of the B register is filtered prior to gating into the adder. The 'filter' consists of true/complement selection gates which are divided into three sections: the most significant bit, the least significant bit, and all the remaining central bits. The output of this filter is the independent result of these sections and may be either all zeroes, all ones, or the true contents or one's complement of the contents of the respective bits of the B register.

The memory information register is the interface to the switch interlock. MIR functions as a buffer to main memory or to a peripheral device. It is an output destination of the barrel switch and its output can be sent to the B-register or the switch interlock.

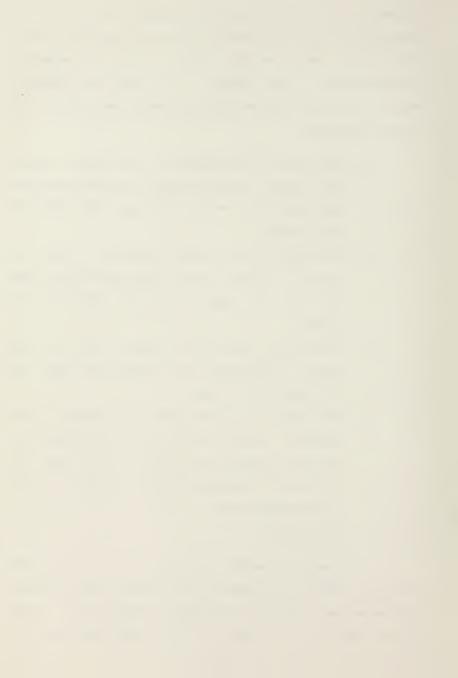
The adder in the logic unit performs all arithmetic functions and can be categorized as a version of a carry look-anead adder. The control unit can gate various combi-



nations of A, B, and Z inputs to the adder. An 'A' input is defined as an input from one of the three scratch pad registers. A 'B' input is the output of the B register's true/complement filter gates. A 'Z' input is an external input to the logic unit and can originate from one of the following sources:

- a. The output of the counter in the memory control unit (MCU) which is gated to the most significant eight bits of the adder with the remaining bits zeroed.
- which is gated to the least significant eight bits of the adder with the remaining bits zeroed.
- c. An optional input which is gated into the middle bytes of the adder with the most and least significant bytes zeroed.
- d. The output of the alternate microprogram count register (AMPCR) in the MCU which is gated into the least significant 12 bits of the adder (13 bits for 8K micromemory machines) with all other bits being zeroed.
- e. All zeroes.

Two inputs, selected from the A, B, or Z sources, are always gated to the adder. These inputs are referred to as X-select and Y-select. An X-select input may be either an A input or a Z input. If it is not specified, it is



assumed to be zero. A valid Y-select has either a B, Z or 1 as its input. Some Z inputs, however, are valid only as Y-select inputs. Any combination of valid X-selects and Y-selects are permissible addends, with an option of adding a one to the least significant bit. For subtraction operations, the value to be subtracted must be a Y-select; the Y-select input is subsequently two's complemented and gated to the adder. All binary Boolean operations between two adder inputs are allowed, and dynamic condition bits for overflow (AOV), all bits true (ABT), and most/least significant bit test (MST/LST) are available to the control unit for testing. Bit testing is a valuable feature for decoding instruction words.

The barrel switch is a matrix of gates that accepts parallel data from the adder and shifts the data any number of places to the left or right with zero fill. It also can right shift the word in an end-around fashion. The output of the barrel switch may be directed to any of the following destinations simultaneously:

- a. The A registers.
- b. The b register.
- c. The memory information register.
- d. The least significant 16 bits to the MCU registers.
- e. The least significant three to six bits to the control unit shift amount register (bit length depending on the word size of machine).



2. The Control Unit

The control unit has five major sections: the shift amount register (SAR), the condition register (COND), part of the control register (CR), the decoder for microprogram memory content, and clock control. This module of the D-machine manages the functions of the processor, and is directly responsible for logic unit operation.

SAR and its associated logic control shifting operations by loading shift amounts into SAR and generating the required controls indicated by the current microinstruction for the barrel switch. In addition, the SAR's logic generates the 'word length complement' of the SAR contents where the complement is defined to be that amount which would restore the bits of a word to their original position after an end-around shift of N followed by an end-around shift of the 'complement' of N. For example, if an end-around right shift of 20 was required in a 32-bit D-machine, another end-around shift of the complement of 20 (12) would be required to restore the contents to its original value.

The condition register has four major functions:

- error indicators, interrupts, status, and
- ing conditional operations. These 16 bits are composed of the 12 condition bits of the



condition register plus the 4 dynamic conditions generated by the LU adder during the present clock time.

- c. It decodes bits from the memory for resetting, setting, or requesting the setting of designated bits of the condition register.
- d. It resolves priority between interpreters in the setting of global condition bits (GC), thereby providing a method of controlling interinterpreter lockout.

The control register stores the control bits of the 56-bit microinstruction that are not being used in the first phase of the execution cycle. The control register is sub-divided into sections which are used by the memory control unit, the logic unit, and the control unit during the execution phase of a microinstruction. For a description of timing and phases, see section C of this chapter.

3. Memory Control Unit

The memory control unit provides the basic addressing interface between the D-machine and both main memory (S-memory) and microprogram memory (M-memory). One MCU can address 64K words (256K bytes) of main memory, and if the D-machine is configured with a second MCU, a maximum of 128K words can be addressed.

The memory control unit has three major sections:



- а. The microprogram address section controls the addressing of microprogram memory and the sequencing of microinstructions. It contains the microprogram count register (MPCR), the alternate microprogram count register (AMPCR), the incrementer, the microprogram address controls register, and their associated logic. standard 4K M-memories, the MPCR and AMPCR are 12 bits long. For 8K M-memories, MPCR and AMPCR are 13 bits in length (the D-machines installed at the Postgraduate School employ 8K M memories). AMPCR is a Y-select input to the logic unit adder.
- b. The memory/device address section contains the 8-bit memory address register (MAR), two 16-bit base registers (BR1 and BR2), output selection gates, and associated control logic. When forming a memory address, the lower eight bits of a base register and MAR are concatenated. The concatenated 24-bit contents of BR1/ BR2 and MAR (BMAR) is a valid Y-select input to the logic unit adder.
- c. The Z register section contains two registers which are Z inputs to the logic unit adder. The literal register (LIT) is an 8-bit register into which constants are loaded. An 8-bit counter (CTR) is used in conjunction with a counter overflow condition bit to control iterative



looping. The Z register section also contains selection gates for the loadable counter and its associated logic.

4. Microprogram memory (M-memory)

A D-machine may have a dual or single microprogram memory scheme. As indicated earlier, the D-machines used in this emulation project had a single microprogram memory, consolidating the microprogram memory and nanomemory into one 56-bit programmable store memory, often referred to as M-memory. Microprograms, consisting of 56-bit microinstructions, are dynamically changeable by the user, thus distinguishing the D-machine as an extremely flexible computing device.

The sequencing of microprogram instructions is controlled by a condition bit procedure which determines the successor command to be executed. M-memory provides data to the condition testing logic which then determines which condition is to be tested. The output of the condition testing logic is a true/false signal that is gated to the successor selection logic. This logic then selects between the three true and three false successor bits also provided by the M-memory word. The three selected bits provide eight possible successor combinations:



- a. WAIT Repeat the current instruction.
- b. STEP Step to the next instruction.
- c. SKIP Skip the next instruction.
- d. JUMP Jump to another M-memory address.
- e. RETN Return from a microprogram subroutine.
- f. CALL Call a microprogram subroutine.
- g. SAVE Step and save the instruction address.
- h. EXEC Execute one instruction out of sequence.

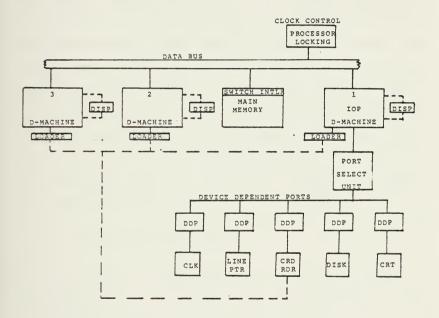
The particular successor command chosen controls gates which select the appropriate M-address from MPCR or AMPCR and provides incrementing logic for generating the next M-memory address. Except for the EXEC command, the MPCK is loaded with this M-memory address.

B. NPS MICROPROGRAMMING FACILITY

1. Physical Description

The Computer Science Department of the Naval Post-graduate School possesses a Burroughs Interpreter-Based System consisting of three interpreters (processors) also known as D-machines, a 64K-32-bit word, main memory module, a card reader, a dual cartridge disk drive, a line printer, and a Datamedia 2500 CRT functioning as a supervisor's console (Figure IV-2). All input and output is performed through a single D-machine processor, hardware configured with device dependent ports (DDP) for peripherals and the external clock.





NAVAL POSTGRADUATE SCHOOL MICROPROGRAMMING FACILITY
BURROUGHS INTERPRETER-BASED SYSTEM

Figure IV-2



After initial light-off and bootstrap, the system is configured into two Burroughs 6700 - LIFO ALGOL Stackmachines, each addressing 32K of memory and each communicating with the input output processor (IOP) in a pseudomultiprocessing environment. Software, written in ALGOL, is provided which runs on the 8-6700 system. A resident monitor control program and disk file manager control the maintenance of system files and the execution of jobs in a batch environment. Both D-machines compete for system jobs input from the card reader or CRT. Other software available includes an ALGOL compiler (a derivative of ALGOL 60), a microprogram translator called TRANSLANG, a line editor, and a simulation program for microprograms. TRANSLANG provides the medium by which microprograms are written. User microprograms loaded into a D-machine change its identity and destroy the Stack-machine previously loaded.

2. Input/Output Interface

Pivotal to the operation of the Burroughs system is the input/output interface. Only one processor, the IOP, communicates with peripherals, and the other D-machines, configured as Stack-machines, must compete for its services. The IOP communicates asynchronously, using a conventional 'handshake' method. Since all interpreters have access to the main memory module, a communications link has been established using the upper two 32-bit words of main memory. If a Stack-machine wishes to communicate with the IOP, it places a message into address 65,535 known as the 'mailbox',



and issues an interrupt (INT) to the IOP. The IOP periodically tests INT, and if set, will retrieve the contents of the mailbox (and mailbox - 1 if required) and perform the desired operation. The other Stack-machine is locked out from interrogating the IOP until it has completed processing the request. Normally, the operation requires transferring a buffer to some output device. When the IOP has completed honoring the request, it places a completion code in the mailbox and sets INT for the Stack-machine requesting the I/O. This interpreter must halt execution and check mailbox to see if the I/O was performed successfully, completing the handshaking process. This protocol permits both Stack-machines to perform input/output independently of each other, provided both maintain strict memory boundaries.

Another function of the IOP is interfacing character code formats between the peripherals and the other two D=machines. When the machines are configured as Stack=machines, characters are passed to the IOP in 6-bit BCL (Burroughs Common Language). The IOP must convert this character set to ASCII for output to the line printer and CRT. A similar translation must be made for input data converting from either EBCDIC or ASCII depending on whether the input source is the card reader or the CRT.

3. Memory Interface

Since all three D-machines must share the 64K of main memory, a priority scheme was developed to resolve



memory reference conflicts. The main memory module is actually a single-ported, 32-bit word, core memory which can be made to appear multiported using a switch interlock unit (SWI) developed by Burroughs. The switch interlock controls the main data bus of the system, and resolves conflicts using a priority scheme. The D-machine with the highest priority is the IOP, with the priority of the other two machines being relative to their physical proximity to the IOP. Once a memory reference has been made, a D-machine may continue execution without waiting for a completion signal from the switch interlock. Although this technique of memory referencing minimizes unnecessary delay, it restricts the program from changing the read or write addresses or the content of MIR (write only) prior to a completion signal.

C. MICROINSTRUCTION TIMING

The Burroughs D-machine initiates a microinstruction once every clock cycle. The D-machines utilized for the AN/UYK-20 emulation operated from a one mHz internal clock, which produced a clock pulse once every microsecond. A D-machine designed with an eight mHz clock, emitter-coupled logic (ECL), and a faster memory cycle time, however, could execute eight times faster. This implies that advances in circuit technology can permit emulations to achieve improved speed and performance with no change in the microprograms.

Every microinstruction is executed using one or more sequential time periods, called phase 1, phase 2, and phase



3. A phase is a constant interval of time equivalent to one clock duration measured from the trailing edge of each successive clock pulse. Some microinstructions only require phase 1 to complete execution. Some require phase 1 and phase 3, and still others require phases 1,2, and 3. A new microinstruction is initiated at each clock cycle, allowing for overlapping of microinstruction execution in phase 1 and phase 3.

Microinstructions consist of two types. In a type 1 microinstruction, events can take place in all three phases:

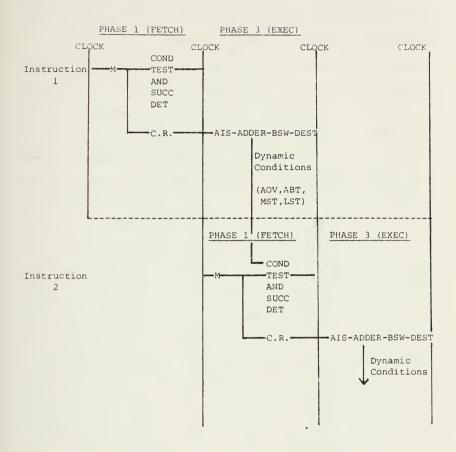
- Phase 1: condition testing, (conditional) external operations or (conditional) logic operation initiation after completion of a prior logic operation, and successor Machine M
- Phase 2: a holding chase for phase 3 logic operation controls.
- Phase 3: the completion phase for logic unit operations and destination register gating specified by logic operation.

During the optional phase 2 period, a type 1 microinstruction execution completion is held in abeyance while a subsequent type 2 instruction is executed. A type 2 microinstruction requires only phase 1 to complete execution, and involves literal assignments to three registers:



next sequential type 1 instruction does not execute its conditional logic operation and therefore can complete its execution in phase 1 (Figure IV-3). Appendix D of Ref. 6 has a complete discussion of microinstruction timing.





M - MPM ACCESS TIME

COND TEST AND SUCC DET - CONDITION TEST AND SUCCESSOR DETERMINATION

BSW - BARREL SWITCH

DEST - BARREL SWITCH JUTPUT DESTINATIONS; I.E., REGISTERS (B,CTR,ETC.)
AND THEIR INPUT LOGIC

C.R. - COMMAND REGISTER AND ASSOCIATED LOGIC

AIS _ ADDER INPUT SELECTION FROM COMMAND REGISTER

Timing Analysis, Type I Instructions

Figure 1V-3 [17]



D. TRANSLANG

Microprogramming on the D-machine is accomplished using microtranslator/assembler called TRANSLANG. TRANSLANG allows the programmer to write microinstructions mnemonically without concentrating on the bit patterns that compose the microinstructions themselves. TRANSLANG is written in ALGOL, the language of the 86700 Stack-machine. Nearly the entire language of TRANSLANG is composed of reserved words recognized by the ALGOL program. Each reserved word has a special meaning which causes the translator to construct particular microinstructions. A TRANSLANG instruction is equivalent to one microinstruction consisting of the set of parallel D-machine functions performed during the clock phases. IRANSLANG is a free form language and instructions may be written in almost any order. Multiple instructions may appear on a line, separated by a period '.'. IRANSLANG constructs include iterative mechanisms, input/output, assignment functions, control transfers, and Boolean, and computational operations. In addition, TRANSLANG permits label definitions and symbolic references for program control flow. Reference 6 is the programming manual for TRANSLANG and contains the complete syntax for the language. Appendix A of Ref. 10 documents additions to the TRANSLANG instruction repertione.

A microprogrammer may construct complicated microinstructions that perform many different tasks, some interacting closely with D-machine clock timing. Microinstruction



gating to several devices permits a single TRANSLANG instruction to accomplish some or all of the following actions:

- a. test a condition.
- b. set/reset a condition.
- c. initiate an external operation.
- d. add.
- e. shift the result of an add.
- f. store the result into several registers.
- g. increment a counter.
- h. complement a shift amount.
- i. determine the successor microinstruction.

By judiciously composing his microprogram, a programmer may minimize execution time by taking advantage of microinstruction phase overlap and using highly parallel microcode.

The TRANSLANG assembler constructs an object program consisting of non-relocatable 56-bit microinstructions. TRANSLANG maintains a cross reference table that resolves label references during assembly. The object code created is stored on a disk and may be loaded into the micromemory of a D-machine using a special control word recognized by the operating system. Once loaded, the D-machine assumes the control structure dictated by the users microprogram.



V. AN/UYK-20 EMULATOR

A. EMULATION DESIGN

1. Functional Components

The architecture of the AN/UYK-20 emulator microprogram was developed using general guidelines provided by references and previous emulation experience on Burroughs D-machines [10]. The first decision incorporated in the emulator design was to integrate the entire emulation within one D-machine. Since the D-machines had the capacity to nandle nearly 8k of microinstructions, no microprogramming capacity limitations were envisioned. The design objectives of a modularized, well-documented, structured microprogram could also be realized.

with the emulator entirely contained in one D-machine, several secondary benefits also existed. First, the emulator was more immune to hardware problems. If one D-machine was malfunctioning, the emulator could still be run on the alternate D-machine. Second, it was possible to have two AN/UYK-20 emulators resident in the system at one time. Not only would two emulators speed up testing of the individual emulation, but they would also permit their eventual use in a system configured for AN/UYK-20 multiprocessing. The third and final benefit of a totally integrated



emulator was recognized during the design of the input/output controller (IOC). Since the AN/UYK-20's IOC was capable of independent processing, an emulation of its IOC would not be possible within the same D-machine. An emulation of the IOC could be accomplished in a second D-machine, which would behave as an independent channel for the D-machine configured as the AN/UYK-20 processor. Although this emulation does not attempt to emulate the AN/UYK-20 IOC, the fact that a second D-machine exists makes its implementation a realistic extension to the project.

The emulator program organization was created following the basic quidelines of Ref. 17. The loader occupied the lowest section of M-memory with the emulator microcode following sequentially. Microprogram control passed from the loader to the emulator via the execution of a 'G' card which signified execution commencement.

The emulator microprogram was organized into three modules positioned such that forward address referencing would be minimized in the TRANSLANG assembler to save time and space. The utilities section was in the lowest portion of the emulator, since its routines were referenced frequently by the succeeding sections. Individual subroutines within the utility section were organized alphabetically.

The instruction and memory fetch routines comprised the next module. These routines incorporated all fetch options available in the AN/UYK-20 emulator.



The opcode routines occupied the last section of the emulator. The opcodes were arranged numerically with further indexing determined by the remaining fields of the individual instruction. Figure V-1 shows the M-memory mapping of the AN/UYK-20 emulator layout. Appendix F contains the emulation program listing.

2. Main Memory Organization

Of primary importance in the emulation design was the logical organization of the Burroughs system's main memory. Since the AN/UYK-20 was a lo-bit word machine, it was decided that only the lower half-word of a Burroughs 32-bit word would be used by the emulator. This design restriction permitted the addressing structure of the AN/UYK-20 to be directly projected on the D-machine. A one-to-one correspondence between the memory address of the AN/UYK-20 and the Burroughs system was also achieved.

Since the number of high-speed registers available in the D-machine was small, a 1K portion of main memory was reserved for the AN/UYK-20 addressable register set, the page address registers, the temporary storage space, and the emulation buffers. The mapping of the AN/UYK-20 high-speed registers to main memory greatly simplified the microprogramming requirements of the emulation, but added considerable execution time overhead. Memory access times for the mapped registers were much slower than the actual transfer



UTILITIES

INPUT/OUTPUT CONTROLLER

FETCH

OPCODE ANALYSIS

0000

		OPCODE	00		 	
1		OPCODE	01			
		OPCODE	02			
		OPCODE	0 3			
	•					
	•			•		
	•			•		
	•	OPCODE	74	-	 	
	•	OPCODE OPCODE		•		
	:		75'	:		

AN/UYK-20 EMULATION ORGANIZATION

Figure V-1



rates of the AN/UYK-20 registers. Figure V-2 shows the complete main memory mapping of the emulation reserved storage area.

3. Emulation Program Status Word

Although the emulation duplicated all the AN/UYK-20 registers, the registers which comprised the program status word (PSW) possessed unique characteristics. Status register 1 was combined with the program address register to form a single 32-bit PSW. The emulator's PSW always co-existed in the A1 register of the D-machine and in main memory during execution of AN/UYK-20 programs. The fields of SR1 were modified to include certain emulator togales, along with the normal condition bits (Figure V-3). The condition bits for DMA and non-destructive read only (NDRO) mode were removed from the SR1 since they were hardware features of the AN/UYK-20 that would not be emulated.

Status register 2, the remaining 16 bits of the AN-UYK-20's PSN, was not resident in any D-machine registers during emulation execution for two reasons: the emulation could not afford the luxury of 48 bits of reserved register space, and SR2 was less frequently referenced than SR1 and the P-register. Consequently, SR2 had to be read from its reserved location in main memory. The contents of the upper 16 bits of SR2's memory location also contained additional emulation toggles which were used by the debugger package (Figure V-3).



MAIN MEMORY MAPPINGS

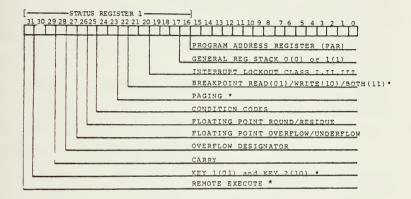
DECIMAL	OCTAL	USF
ADDRESS	ADDRESS	
*****	*****	********
0 - 15	0 - 17	GENERAL REGISTER STACK 1
16 - 31	20 - 37	GENERAL REGISTER STACK 2
32	40	PROGRAM STATUS WORD
3 3	41	BREAKPOINT REGISTER
34	42	STATUS REGISTER 2 (SR2)
35	43	NEXT LOAD ADDRESS
36	44	CLOCKTIME
57	45	REAL TIME CLOCK
38 - 43	46 - 53	WORKSPACE (TEMP STORAGE)
44 - 49	54 - 61	STACK (TEMP STORAGE STACK)
50 - 53	62 - 65	I/O COMMAND WORDS (IOCW)
54 - 119	06 - 167	UNUSED
120 - 121	170 - 171	HEX ADDRESS FOR INPUT
122 - 141	172 - 215	INPUT CARD BUFFER
142 - 152	216 - 230	UNUSED
153 - 185	231 - 271	OUTPUT PRINT BUFFER
186 - 205	272 - 315	CRT BUFFER
206 - 229	316 - 345	ERRORLIST
230 - 767	346 - 1377	UNUSED
768 - 1023	1400 - 1777	PAGE ADDRESS REGISTERS

Figure V=2

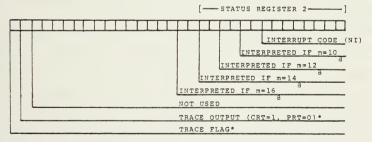


AN/UYK-20 EMULATION PROGRAM STATUS WORDS (PSW)

ACTIVE PSW: RESIDES IN LU REGISTER AL (MEMORY ADDRESS 32)



INACTIVE PSW: RESIDES IN MEMORY ADDRESS 33



* FIELDS ADDED FOR USE BY THE EMULATOR

Figure V-3



4. D-Machine Registers

with only a limited number of high-speed registers available in the D-machine, the emulation design had to include a well-developed plan for their usage. Since only seven registers in the D-machine were 16 bits or longer, they were used exclusively for manipulating the AN/UYK-20 addresses, instructions, and data. The register environment had to be consistent throughout every execution cycle to allow utility routines to be called in the same manner by all opcode subroutines. The primary goal of the emulation was to use as few memory references as possible to conserve execution time and memory space. Judicious use of the existing registers was a necessity.

Several factors had to be considered before selecting a register for a particular function. The most important consideration was its flexibility within the D-machine. The B register, for example, was used as a general purpose register, since its contents could be gated through a masking filter prior to being utilized. A second factor was the type of operand it could contain. Double-word operands (32-bit) could only be stored in the 32-bit logic unit registers while 16-bit operands could also be stored in the

The All register contained the emulation's 32-bit program status word (PSW) at the commencement of the emulator program. It was not affected by individual instruction



microcode, except when incrementing the PAR, or when a particular instruction modified the PSW. Emulator toggles resident in SR1 could not be altered by an AN/UYK-20 instruction because their settings were independent of program execution.

The A3 register held the instruction word for the duration of its execution cycle. Each field of the instruction could be decoded and interpreted from the A3 register without having to retrieve it from memory. Once the instruction had been completely decoded, A3 was made available as a scratch pad register.

The A2 and B registers were used as scratch pad registers during each opcode execution cycle. In general, their contents were volatile, except when they were specifically documented in the the program listing. The contents of A2, for example, was not altered in the EMULIN subroutine, because of its use in the calling fetch routine. A2 and B were manipulated as either single or double-word operands during the arithmetic operations.

The only remaining logic unit register was the memory information register (MIR). MIR was used for storing information into memory and as a temporary storage location. Intermediate results were deposited in MIR during instruction execution and returned through the B register.

The base registers, BR1 and BR2, were used as storage for addresses and single-length operands, and for



temporary storage of intermediate results. In addition, all memory addressing in the emulation was accomplished using the lower 8 bits of BR2 and MAR (MAR2). These memory control unit registers had to be used carefully, because they required a sequence of several microinstructions to properly reference their contents.

B. LOADER

The loader incorporated into the AN/UYK-20 emulation provided a simple mechanism for loading AN/UYK-20 instructions into main memory (S-memory) of the Burroughs microprogramming system (Figure V-4). Its control word repertoire was flexible, allowing a variety of AN/UYK-20 program environments. Job control statements were included to execute and halt individual programs anywhere in S-memory.

The loader module consisted essentially of a scanner and a translator written in the microcode. Information was read into a 20-word buffer from cards or CRT input, then the buffer contents were scanned for control code consisting of one or more characters. Once these characters were interpreted, control was passed to the translator section which decoded the rest of the data in the buffer and performed the required function. The translator section consisted of a variety of routines that handled specific control words in the loader repertoire. The loader control statements, however, had to appear in a logical sequence (See Appendix A).



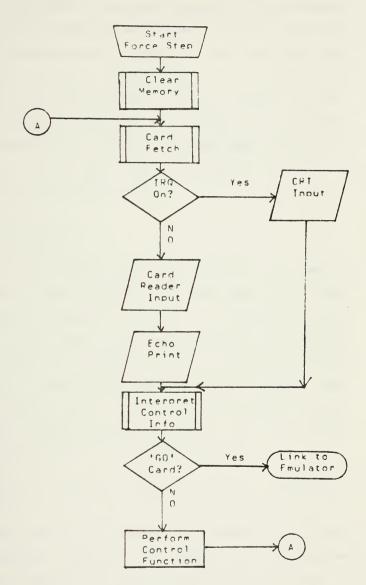


Figure V-4



The actual interface pipeline between the loader and the emulator consisted of two small emulator utility routines which started and stopped the external clock of the Burroughs microprogramming system. These routines were inserted for emulation timing purposes, and provided a 'stop watch' for AN/UYK-20 programs. The time recorded (in milliseconds) by this 'stop watch' was placed in a reserved memory location in the emulation memory map, and could be read using either a trace control instruction ('I'), or a machine status control word ('M').

C. THE FETCH MODULE

In order to emulate AN/UYK-20 execution and memory referencing, fetch microcode was developed which incorporated memory addressing algorithms and instruction fetch routines. Since both data and instructions were equally accessible from the processor, the memory addressing scheme was closely linked to the instruction fetch concept. Data and instructions could be interspersed throughout memory, and proper program execution required that the program address register point to an instruction word.

The emulation used two routines for memory addressing, EMULIN for reading, and EMULOUT for writing (Figures V-5, V-o). These subroutines performed both paging and breakpoint checking, depending on toggles set in the program status word. Paging was incorporated into the emulation in order to gauge the execution overhead required in emulating



the AN/UYK-20's pading scheme. The paging scheme implemented in the emulator divided main memory into 256-word pages, instead of 1024-word pages used by the AN/UYK-20. Since the Burroughs D-machine was organized for 256-word pages, the microprogramming required for the paging was straightforward. The 256 page address registers resided in the emulator's memory mapping, each initialized to the page number corresponding to their relative address (0-255). The paging algorithm imitated the AN/UYK-20's method of page addressing, and included the setting of a page modification bit.

The breakpoint option was added to provide a method of debugging AN/UYK-20 programs, once the emulation was completed. EMULIN and EMULOUT tested toggles set in the PSW to determine if breakpoint read, write, or both was desired.

The memory addressing convention required all memory references from 1K to 64K to use EMULIN and EMULOUT. All memory references to the memory mapping area (0-1023) did not use these routines, but instead utilized absolute memory referencing microcode.



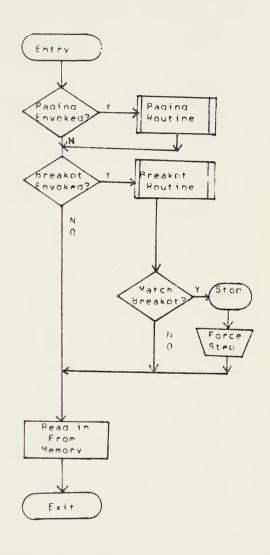
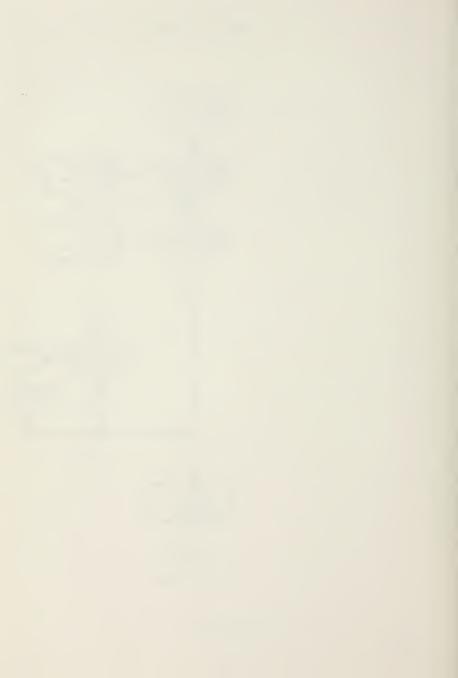


Figure V=5



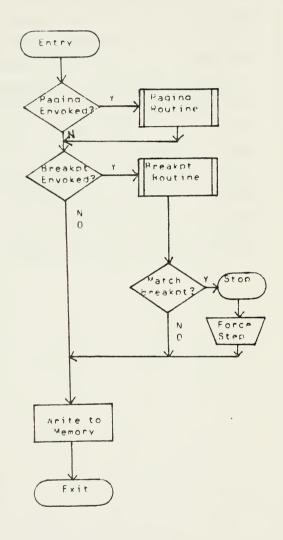
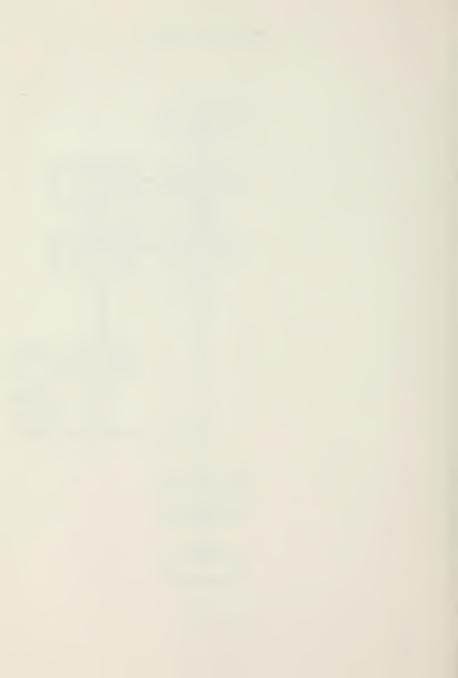


Figure V-6



The instruction fetch routine (IFETCH) retrieved instructions from main memory based on the contents of the program address register. Since IFETCH used EMULIN to read the instructions from memory, it could operate in a paging environment, with or without breakpoints (Figure V-7). IFETCH was also responsible for incrementing the PAR, and for testing the trace toggle prior to fetching an instruction. IFETCH was carable of retrieving any instruction word in the program address space (1024-65,535). In the event that the upper memory limit was reached, IFETCH would set the PAR to 1024 and continue execution. Trace toggle testing was inserted into IFETCH as part of the puilt-in debugging package. Since IFETCH was called prior to every instruction, it was the logical choice for placing a call to the debugger.



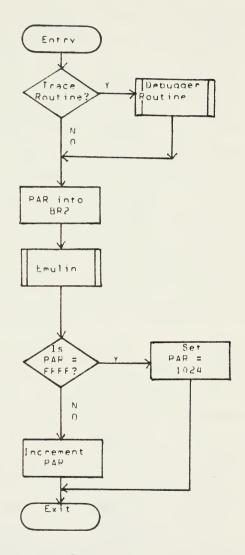
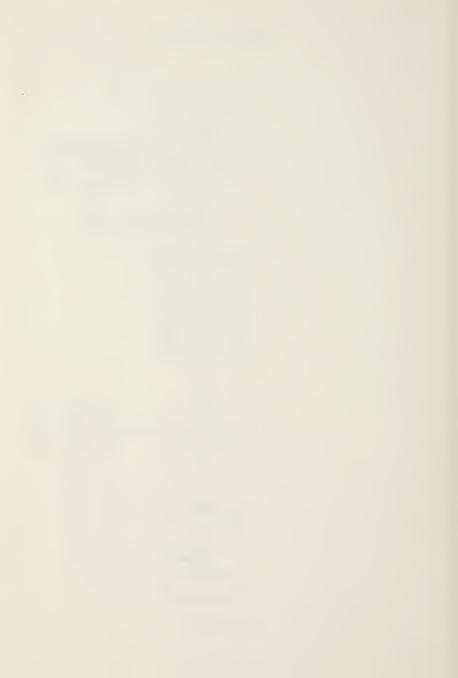


Figure V-7

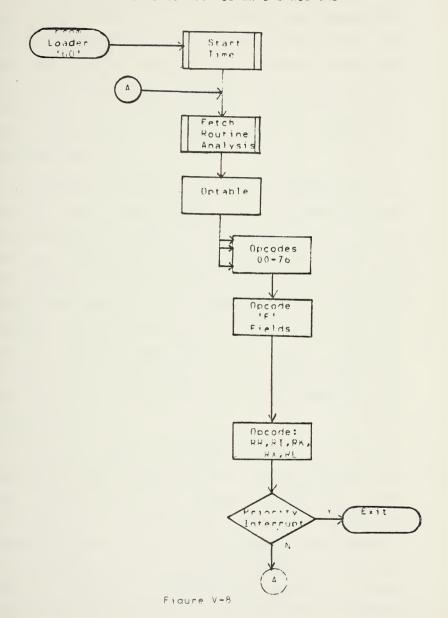


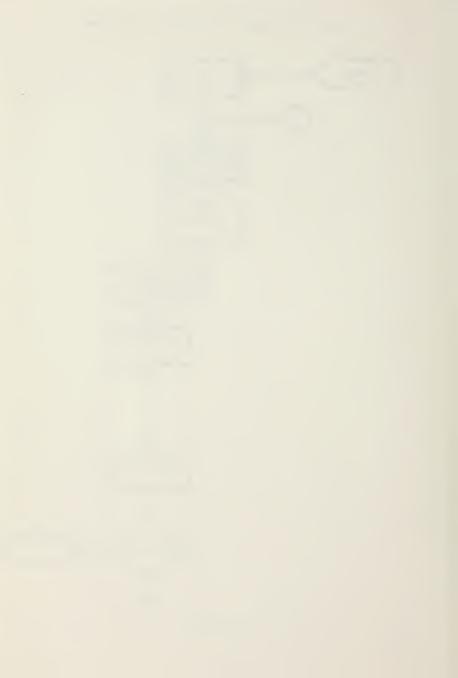
D. OPCODE IMPLEMENTATION

All of the 205 individual instructions emulated were microprogrammed using an identical instruction decoding mechanism. The routines that performed the required operations were terminal nodes on a large tree network, whose root was the OPCODE routine. OPCODE fetched an instruction and isolated the operation code field. The binary value of the opcode field was an index to an operation jump table containing individual occode M-memory addresses. Within each opcode routine was microcode which isolated the subfunction 'f' field of the instruction and used its value as an index to the next level of opcode analysis. Depending on the opcode, this last jump could identify which instruction was to be performed. If it did not, further analysis of the 'm' or 'a' fields provided the final index to the instruction. Instruction formats are described in Appendix C.

After the instruction had been executed, control passed back to the opcode routine, and then the execution cycle was repeated for the emulation of the next AN/UYK-20 instruction. The AN/UYK-20 programmer could cause this microprogram loop to be exited by either inserting an executive return instruction (03,0,a,00) which caused a 'priority interrupt' and halted program execution, or by coding an instruction that was not implemented, not assigned, or caused a division overflow. The last three cases caused an execution fault, while the former resulted in normal program termination (Figure V-8).







The instruction fetch mode of OPCODE assumed that the PAR always pointed to an instruction word. Double-word instructions always had their 'y' field fetched after they were determined to be two words in length. Conditional double-word instructions performed their condition test before the 'y' field was fetched. If the test failed, the PAR was incremented by two prior to returning to OPCODE for continued execution.

The OPCODE routine was also written to accommodate the AN/UYK-20 'remote execute' instruction. When this operation was performed, a bit was set in the PSW which would indicate that one instruction out-of-line was being executed. For this operation, the current PSW was stored in memory, and the PAR was loaded with the address of the instruction to be executed. The OPCODE routine always checked the remote execute bit during an instruction cycle. If the bit was set, it would fetch the instruction indicated by the remote execute PAR, and restore the actual PAR, incremented by two, into the PSW.

Some of the opcode repertoire of the AN/UYK-20 was not emulated. Those instructions that were not emulated, however, retained slots in the opcode hierarchy for future inclusion. Any instruction not implemented by the emulator caused the machine to fault, and printed an error diagnostic on the selected cutout device ('NOT IMPLEMENTED = EXECUTION ENDS '). Similarly, locations were reserved for those instructions not assigned by the AN/UYK-20 were reserved



locations in the emulation. This permitted the emulator to be responsive to any future AN/UYK-20 hardware modifications. Whenever an instruction to be executed was not assigned, the emulator generated a fault interrupt and printed an error diagnostic on the selected output device ('FAULT INTERRUPT - EXECUTION ENDS').

E. UTILITIES

Although each emulated instruction performed different operations, each depended upon a common set of utility subroutines to accomplish their task. These subroutines varied in complexity, but each performed a function that contributed to successful instruction execution. A simple operation often required register addressing, condition code setting, and memory addressing, pefore the task was completed.

Utility subroutines were included in the emulation whenever feasible to simplify microprogramming and to alleviate programming redundancy. These subroutines were called using the successor command constructs available in TRANSLANG. Depending on the purpose of the utility routine, parameters were passed via D-machine register(s) or condition bit(s). This information was utilized by the utility in determining what operation was to be performed. In the carry subroutine, for example, a local condition bit was passed which indicated the appropriate condition code to be inserted into the PSW. A more complex example, the RX



format utility routine, required two parameters to be set by the instruction. Register A3 contained the instruction word and LC2 was set or cleared depending on whether or not byte formatting was required. The RX routine called other routines and could perform considerable processing before the final result, the effective operand address, was returned to the calling routine via the B register.

The utility section encompassed a number of routines which performed complex data manipulation. Arithmetic utilities for multiplication, division, and square root were accessed by nine separate AN/UYK-20 instructions. Indirection routines, which were called by the PX format routines, emulated the AN/UYK-20 cascaded addressing capabilities. A general purpose move subroutine permitted up to 256 cells of main memory to be moved from one location to another. This routine was used by the emulator's error diagnostic utilities, as well as the load and store multiple address register instructions.

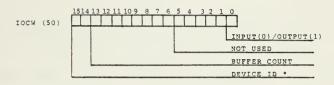
F. INPUT/OUTPUT CONTROLLER

Although the AN/UYK-20's IOC was not emulated, several of its design features were imitated in creating a general purpose input/output controller for the emulator. The input/output command instruction (35 RR) initiated the I/O sequence, and reserved several cells in the memory mapping for I/O control words (Figure V-9). These control words contained fields which indicated what peripheral device was



AN/UYK-20 EMULATION

INPUT/OUTPUT COMMAND WORDS



IOCW + 1

BUFFER ADDRESS
THE MICROCODE ALTERS THE IOCW + 1
DURING BUFFER TRANSFER

IOCW + 2

BUFFER SIZE USED FOR CRT OUTPUT

IOCM + 3

NUMBER OF SECTIONS
USED FOR DISK TRANSFERS (NOT IMPLEMENTED)
* CODE: 00 - CRT
01 - PRT (OUTPUT)/CRD RDR (INPUT)

10 - DISK (NOT IMPLEMENTED)

Figure V-9



selected, the number of buffers that would be passed, whether input or output was desired, and where the buffer was located. Two additional words were reserved for control data required to interface with the disk and the CRT. The disk input/output microcode was not incorporated into the controller, but the framework was provided so the IOC could be readily inserted in the future.

The emulator's IOC section was located in the utility section of the emulation, and operated asynchronously with the Burroughs IOP. Since the IOC was collocated with the emulator in the same D-machine, it was not capable of independent processing. Once it was initiated, emulation execution waited until input/output was completed. The emulation had to use the Burroughs Common Language, since the IOP was microprogrammed to accept only this character set from other D-machines.

In order to transfer a 33-word line printer buffer to the IOP, the AN/UYK-20 emulator IOC had to use 66 AN/UYK-20 words. In order to send 20 words to the CRT, the IOC had to contruct a 40-word buffer. The COMPRES subroutine packed an AN/UYK-20 buffer of 66, 16-bit words into a 32-bit, 33-word buffer, suitable for output to the IOP.



Similarly, on input, a 20-word IOP buffer from the card reader or CRT expanded into a 40-word AN/UYK-20 buffer. In this case, the EXPAND subroutine split every packed 32-bit word of the IOP's buffer into two 16-bit words, suitable for processing by the emulator. These additional data transformations were required because of the buffering requirements of the Burroughs IOP.



VI. EMULATION TESTING

A. METHOD OF TESTING

The fundamental testing technique utilized throughout the development of the emulation consisted of three distinct phases: 1) each module was independently assembled and debugged until successful assembly was achieved, 2) each program segment was then tested for accuracy of the intended operation, and 3) the composite emulation program was tested under actual program conditions allowing for interaction among several modules. A debugging package, which was developed early in the emulation project, was the primary test vehicle for verifying emulation coding. Development and testing of the loader was, however, completed prior to the creation of the debugger.

Loader testing was accomplished by monitoring the control panel lights and synthetically halting program execution via the insertion of 'WAIT' statements, forcing the desired register to be transferred to 'MIR', and then reexamining the panel lights. This process was extremely tedious and time consuming but proved to be an invaluable tool for recognizing peculiar TRANSLANG constructs and microinstruction execution side effects.



Each module was subjected to an extensive desk checking process in order to reduce trivial assembly errors before running it on the machine. After a successful assembly had been achieved, the code was merged with previously existing assembled modules. The emulator was expanded as more modules were added, with utility routines being incorporated prior to the opcode programs.

Initially, the loader was designed, programmed, and thoroughly tested prior to the microprogramming of any. AN/UYK-20 instructions or utilities. With the loader implemented, the emulation of the UYK-20 instruction repertoire could procede with a minimum of loader induced problems.

Independent opcodes and various utility routines were added to the previously assembled programs. The final emulation consisted of a total of 205 opcodes, a set of utility programs, and a workable loader.

In the next phase of testing, every module was subjected to a representative number of test cases which demonstrated how closely they compared to the documented AN/UYK-20 operation. Artificial environments were created to subject every opcode to a variety of situations. Whenever the operation of the opcode disagreed with the documented AN/UYK-20 operation, the opcode's function was thoroughly researched. The opcode's side effects were categorized and questions formulated. Often the answers could only be obtained from the Univac field engineer.



To illustrate the complexity of testing, an add instruction was tested with numerous operand combinations: two positive operands, two negative operands, one of each sign yielding a negative result, opposite signs producing a positive result, and opposite signs producing a zero sum. During each addition operation, the overflow, carry, and condition bits had to be monitored in status register 1 to verify their appropriate setting. This level of detail was achieved with all of the implemented opcodes in order to produce an efficient and accurate emulation.

Throughout the entire testing scenario, which composed 20% of the emulation project, the debugger routine (DUMPREG) provided the necessary information for examining opcode execution. A representative sample debugger output is provided in Appendix D.

DUMPREG permitted a snapshot of both AN/UYK-20 general register stacks, PSW, SR1, and SR2, in addition to the D-machine registers (A1, A2, A3, BP1, AMPCR, MIR) and the Burroughs external clock. DUMPREG possessed sufficient flexibility to be incorporated into the microcode at any point. In the final emulator, however, the debugger is user specified, and will dump the AN/UYK-20 emulator environment either at every instruction fetch and program stop, or when called by a loader control card.



B. SAMPLE TEST PROGRAMS

After subjecting the entire emulation to extensive testing, some representative test programs were developed to demonstrate the feasibility of the emulation and its capabilities and performance as compared to an actual AN/UYK-20. There were two programs which were selected because they incorporated numerous emulation features. The two programs were the solution of simultaneous linear equations by Cramer's rule and generation of prime numbers. It must be noted that streamlined program design was not emphasized but rather utilization of a variety of opcodes and features of the emulation.

The program for solving linear equations contained a total of 28 opcodes, requiring 28 opcode execution cycles and 43 instruction fetches. The program demonstrated all four fundamental mathematical operations, numerous store and load functions, a comparison test and a jump instruction. The capability of performing card reader input and output was added when the emulator IOC was completed.

The prime number program demonstrated 30 instructions which required 116 opcode execution cycles, and 122 instruction fetches. This program illustrated numerous comparison tests, looping structures, several jump instructions, a load multiple instruction, addition, and division. The test programs are included in Appendix E.



C. TEST RESULTS

The performance analysis of the test programs consisted primarily of running numerous test cases, examining the results for accuracy and computing the total time required to execute the emulated AN/UYK=20 programs. The timing of the programs was accomplished by using an external clock available on the ICP. The clock time provided a fairly close representation of the emulation execution time, but it cannot be considered a completely accurate measure since the emulation must interrogate the IOP to retrieve the external clock contents. Approximately 50 microseconds are used when sampling the clock.

The time requirements of the AN/UYK-20 program execution were hand-calculated by summing the published instruction execution times as presented in Ref. 21. The emulation performance ratio (EPR) was computed merely to give an approximate indication of the emulation performance. The EPR is the ratio of measured Burroughs emulation time to the calculated AN/UYK-20 execution time. Two EPR figures are recorded: one with paging implemented and one without. The paging EPR figure is significant only in that it indicates how much additional overnead must be incurred when emulating the paging mechanism of the AN/UYK-20. The required additional execution time was about 26%. Naturally, paging overhead is directly proportional to the number of instruction fetches or memory references performed during a program.



The results of program testing are as follows:

	CRAMER'S	RULE	PRIME NUMBERS
Number of Opcodes	85		30
Number of Fetches	43		122
Execution Cycles	28		116
Time w/o paging	5000	usec	13000 usec
Time with Paging	8000	usec	17000 usec
AN/UYK-20 Time	78	usec	193 usec
EPR w/o Paging	64 ::	1	67 :: 1
EPR with Paging	103 ::	1	88 :: 1

•••••

These figures represent only approximate comparisons of the two machines. These computations provide an estimate of emulation characteristics. An effective EPR without paging was projected to be 65::1.



VII. SUMMARY AND RECOMMENDATIONS

A. EXPERIENCE WITH HARDWARE

The emulation project provided the unique opportunity of learning about two computer systems. The Burroughs D-machine demanded a detailed knowledge of hardware operation, as well as a thorough understanding of the microprogramming language, TRANSLANG. The computer architecture and processor capabilities of the AN/UYK-20 had to be investigated and then integrated into the control store memory of the Burrough's D-machine.

On several occasions, hardware malfunctions with the Burroughs equipment prevented normal system operation. The card reader was inoperable for several weeks, and the disk drive unit had to be repaired several times. During the final three weeks of project development, one D-machine ceased to function properly. This restricted emulation testing to the remaining D-machine.

Although these hardware difficulties impeded normal progress of the project, they did not prevent the emulation from successfully being completed. If a hardware problem prevented emulation testing or debugging, other modules were designed and testing was postponed. This permitted continual emulation development regardless of the hardware



status. In addition, considerable time and effort was invested in trouble-shooting hardware malfunctions, so they could be isolated, diagnosed, and repaired.

B. LESSONS LEARNED

The emulation project brought together many different computer science techniques and disciplines which will be useful in future computer science endeavors. A great deal of experience in both computer architecture and operation was gained in two different types of computers. Microprogramming provided new insight into computer design and revealed many potential applications for programmable control store machines.

Since emulations normally require a large development effort, this project had to incorporate judicious system design and project management principles in order for it to be completed successfully. Careful monitoring of critical stages of the emulation, and coordination of the programming effort to meet scheduled requirements, was necessary throughout this research. The small programming team concept proved to work extremely well in this project.

Finally, several software practices were strictly followed that proved to be invaluable in constructing the emulation. First, modular programming succeeded in partitioning the emulation into discrete modules which could be
designed, coded, tested, and implemented individually. The



emulation was constructed in segments, using the previously verified modules as a test bed for the new modules being built. Structured programming and prolific documentation were useful in developing each microprogram routine because they permitted each team member to understand the function of the program and how it could be used.

C. EMULATION PROBLEMS

The most significant problem of the emulation was not having had any experience with an AN/UYK-20 and not having anyone readily available with prior AN/UYK-20 experience. This lack of knowledge created some anxiety when attempting to analyze the ramifications of individual opcodes.

The idiosyncrasies of certain opcodes were not made self-evident by the AN/UYK-20 software manuals. Consequently, numerous code modules were redesigned when more detailed information was provided by a UNIVAC field engineer. This proved to be very time consuming, inefficient, and frustrating.

Another emulation difficulty was the lack of working registers in the host machine as compared with the target machine. While the AN/UYK-20 has either 16 or 32 general registers, depending on whether the second stack option is incorporated, the D-machine has effectively only seven workable registers containing 16 bits or more. Therefore, all AN/UYK-20 registers had to be mapped into S-memory which



created much longer register read/write times. This created significant register manipulation problems which in some cases required main memory references for instructions intended to be strictly register-to-register operations. Consequently, increased execution times resulted in a higher emulation performance ratio (EPR), decreasing the overall emulation performance.

D. RESULTS

Emulating the AN/UYK-20 on a Burroughs D-machine required a considerable amount of preparation and planning before any results were realized. An in depth analysis of each computer's architecture and operating characteristics was conducted to insure that an emulation was feasible in the allotted time period. From the inception of the project, the goal of the emulation was to implement a standard AN/UYK-20 processor. This decision was based on the capability of the D-machine and an estimate of how much time would be involved in developing, debugging, and testing the final product. Although this goal was achieved, it was felt more time could have been devoted to testing and verifying emulation operation.

The AN/UYK-20 emulation was a highly complex microprogramming project involving numerous data structures and transfer protocols. A total of 205 AN/UYK-20 instructions were emulated out of nearly 290 instructions in the repertoire (including all IOC, math pac, and clock interrupt



opcodes). AN/UYK-20 diagnostic programs and user programs will establish the validity of the emulator's construction.

E. RECOMMENDATIONS AND FOLLOW-ON TOPICS

Although 205 opcodes have been implemented, tested, and developed into a working emulation, there are still many challenging avenues to pursue in creating the complete emulation package. First, testing is a continuous process and should be performed in conjunction with code optimization. A comprehensive code optimization effort could improve the EPR without sacrificing code readability.

Second, the floating point and 'math pac' options could be implemented. The addition of floating point arithmetic, trigonometric, and hyperbolic functions would significantly strengthen the scientific capabilities of the emulation. This would be an extremely strengous undertaking but would permit more tactical data applications of the emulation, increasing its value to the Navv.

One area which could be examined is to perform a comprehensive timing analysis between an AN/UYK-20 and the emulation. This could consist of collecting numerous bench mark programs from Navy AN/UYK-20 installations, where performance data could be accurately obtained. These programs could then be run on the emulator, and analyzed with the pench mark results. The feasibility of replacing or substituting emulation host machines for target machines could be



addressed and supported by the timing analysis study.

An emulation of the AN/UYK-20 input/output controller could be incorporated into the emulation without serious difficulty. Since a second D-machine is available, the IOC channel processor instructions could be emulated and inserted into that D-machine's control memory. The independent processing characteristic of the AN/UYK-20 IOC would be fulfilled using this arrangement.

Finally, when the Burroughs system is linked with the computer science department's PDP 11/50, the AN/UYK-20 emulator could be connected to that system's peripheral resources. This would allow future incorporation of an AN/UYK-20 ULTRA assembler and a CMS-2M compiler into the PDP 11/50 system which could then produce machine language object code files for the AN/UYK-20 emulator to execute.



APPENDIX A. AN/UYK-20 EMULATOR USER'S MANUAL

This description is designed to provide sufficient information to operate the AN/UYK-20 emulation program. It is assumed that the informal Burroughs D-machine manual in the Burroughs laboratory will supply adequate power-on instructions and solve any hardware operating difficulties which may arise.

The procedure for utilizing the AN/UYK-20 emulator can be divided into four phases:

- selection of the necessary loader control cards (JCL).
- 2) selection of the AN/UYK-20 program instruction set.
- implementation of phases one and two into the required card or CRT format.
- 4) actual hardware implementation on the Burroughs
 D-machine resulting in program execution.

Phase one can be achieved by selecting the desired loader control cards described in Appendix B. The card format is identical to the CRT format, except that the CRT requires the user to <carriage return> at the end of every line of input data.

Phase two is accomplished by creating the AN/UYK-20 program from a subset of the 205 emulated instructions.



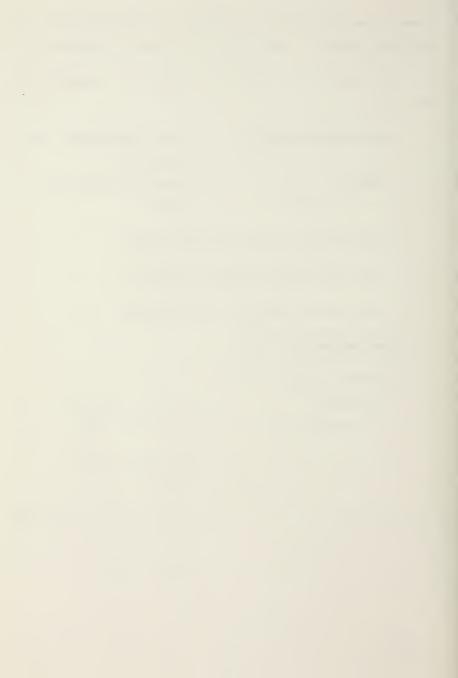
Phase three consists of keypunching the desired JCL and AN/UYK-20 program in the format illustrated in Appendix C.

The resulting job deck will typically be assembled as follows:

?SMLOAD TED/UYK20-OBJECT % loads the emulator into micromemory 00004 % load the program into page 4 C 00206 FAULT INTERRUPT-EXECUTION ENDS " 00214 NOT IMPLEMENTED-EXECUTION ENDS " C 00222 DIVIDE OVERFLOW - FAULT ENTERED" other desired JCL ******* AN/UYK-20 Program 03,0,a,00 % priority interrupt (a = 00-17 octal)(mandatory card) G % commence program execution % machine status (req. dump V (or M1) at termination)

% end job card

Ε



Finally, phase four consists of the entire program deck being loaded into the card reader. It is assumed that the IOP is at address 0015 hex, the selected interpreter is at address 0549 hex, the line printer is 'READY', and the IRQ switch is 'off'.

The IRQ switch is a three-way toggle switch mounted on the right side of the interpreter. In the up position, IRQ is 'on', horizontally it is 'off', and the downward position is used for external functions.

If either the interpreter or the IOP is not at the proper starting address, clear them by depressing the 'CLEAR' button on each unit. If this procedure does not remedy the situation, consult the user's manual in the laboratory.

Upon reading the ?SMLOAD card, the system will load the AN/UYK-20 emulator object program into the micromemory of the selected interpreter. The program address counter (on the interpreter) will be at the beginning of the emulation program, address 0000 hex. At this point, the user can select CRT input and output by placing the IRQ switch to the 'on' (upward) position. If CRT input is not desired, leave the IRQ switch in the 'off' (horizontal) position. Next, force step the interpreter by momentarily depressing the FST button (uppermost push button on side panel of the interpreter). Do not hold in the FST button. This may cause some undesirable side effects.



After depressing the FST button, the AN/UYK-20 program is loaded into S-memory. If the input is expected from the CRT, the user must enter his program from the console. Otherwise, the emulator will request cards from the card reader. Once the program has been loaded and the 'G' card read, program execution begins.

After successful program termination, the program returns to the loader and asks for more input. At this point, the user may terminate his job, or start another load sequence. It should be remembered that the AN/UYK-20 emulator has been designed for monoprogramming execution. It executes one program at a time, but can execute any number of programs in sequential order if desired. When the job is terminated, the D-machine returns to its starting address (0000 hex) and awaits further processing. When the user returns to the start address, the system is effectively 'master cleared' since S-memory will be cleared prior to executing any further jobs. It is not necessary, however, to use the ?SMLOAD card for additional programs or program re-runs because the emulator object code still resides in micromemory.

If the results of program execution are not as anticipated, use of either a 'I' or 'Il' option (trace card) is recommended to provide the user with a fetch-by-fetch program trace with the output to the printer or CRT respectively.



APPENDIX B. LOADER CONTROL CARD FORMATS

CARD COLUMNS

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16 -	- 20
В	R W B		de	cim	al	ad	dr									
С			de	cir	al	ado	dr	ch	arac	ter	stri	ng f	0110	wed i	оу а	11
D			de	cim	al	ade	dr								da	ata
ε						_										
G			de	cim	al	add	o r									
I	1 2					re										ata
L			de	c .	page	e ni										
M	1															
Р																
Б					nur		r									
S	1 2															
T	1															,

Note: All numeric fields are in decimal.



Control Card Identitifier	Description
8	The 'B' card is used to implement the breakpoint feature of the emulation. This features allows the user to specify a decimal address in columns 4-8. Column 2 must contain a R or W to breakpoint on a read or write operation respectively. The default condition is breakpoint on both read and write.
C	The 'C' card is used to insert character strings into memory. The character string starts in column 9 and continues until terminated by a quote symbol (") or the string reaches column 80. The decimal address where the character string will be written is given in columns 4-8. A blank or zero address field causes the character string to be inserted at the current load address.
D	The 'D' card is used to store decimal data from columns 16-20 into the memory address found in columns 4-8. A blank or zero address field causes the data to be inserted at 'the currrent load address.
E	The 'E' card is used to indicate the end-of-job and therefore is a mandatory control card for job separation.
G	The 'G' card or 'GO' card is used to start execution. The starting decimal address is in columns 4-8. The default value of a blank or zero address field will cause program execution to start

adoress 01024.



- I --- The 'I' card or set index register card is used to store decimal data from columns 16-20 into the register designated in columns 7-8, into the general register stack (1 or 2) specified in column 2.
- The 'L' or load card is used to partition memory into 256, 256-word (32-bit) pages and to load the program into the decimal page as referenced by columns 4-8. Pages 0-3 should not be used because they contain the required emulation register mapping and established workspace. The 'L' is a required control card, and it is recommended that it be the first JCL card.
- The 'M' card or machine status card provides a register dump, whereever it is inserted. It is normally placed between the 'G' and 'E' cards in the JCL deck. If a 1 is placed in column 2, the machine status dump will be sent to the CRI. This dump will contain the current value all AN/UYK-20 general registers, the PS%, SR2, next instruction address, the breakpoint address, and clocktime.
- P --- The 'P' card is used to implement paging.
- P --- The 'R' or reserve space card is used to reserve memory space as specified decimally in columns 4-8.
- S --- The 'S' card is used to simulate setting of the program stop switches (1 and 2) on the AN/UYK-20 maintenance panel.

 Column 2 must contain a 1 or a 2. Two cards are required if both switches are to be set.
- The 'I' or trace card provides a fetchoy-fetch program trace, dumping the entire machine status on every fetch cycle. If a 1 is in column 2, the trace will be displayed on the CRI. This card is recommended for debugging programs.



APPENDIX C. AN/UYK-20 EMULATOR INSTRUCTION FORMAT

Format Card Columns ********** 5 6 7 8 9 10 11 12 13 14 RR, RL, opcode, 'f', 'a', 'm' RI Type 2 5 6 7 8 9 10 11 12 RI Type 1 opcode, 'f', d 5 6 7 8 9 10 11 12 13 14 15 16 - 20 opcode, 'f', 'a', 'm', 'v' RK, RX Notes: 1) All fields are in octal with the exceptions of addresses and the 'v' field which are decimal 2) All fields must be zero-filled 3) The following field restrictions must be followed: Field Range Base 0.0 - 76Opcode octal 141 0 - 3 octal 'a' 0.0 - 1.7octal

0.0 - 1.7

000 - 377

00000-65535

00000-65535

octal

octal

decimal

decimal

* m *

101

1 0 1

addr

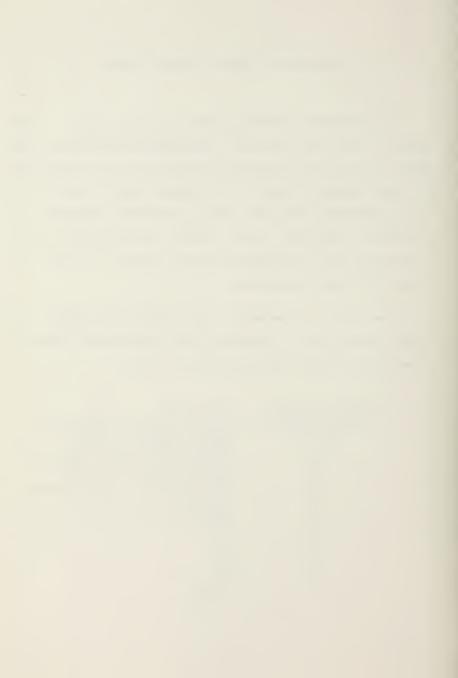


APPENDIX D. SAMPLE DEBUGGER OUTPUT

This appendix provides a sample program output illustrating the Trace option. The debugger is called at the beginning of every instruction fetch, and at the termination of the program. Space has been provided for dumping 48 memory addresses including emulated AN/UYK-20 registers and D-machine registers. Each output line consists of eight regions printed in hexadecimal with a total of eight hex digits (32 bits) per region.

The listing is annotated to indicate the identity of each output cell. A summary of cell definitions (numbering from left to right, top to bottom) follows:

DECIMAL ADDRESS	DESCRIPTION
*******	* * * * * * * * * * * * * * * * * * * *
0 - 15	General Register Stack 1
16 - 31	General Register Stack 2
32	Program Status Word (PSW)
33	Breakpoint Register (BREAKPT)
34	Status Register 2 (SR2)
35	NEXTINSTR (next load address)
36	Clocktime
3 7	Real-Time Clock (RTC)
38	AMPCR
39	A 1
40	SA
41	А 3
42	MIR
43	BRI
44 - 47	Unused



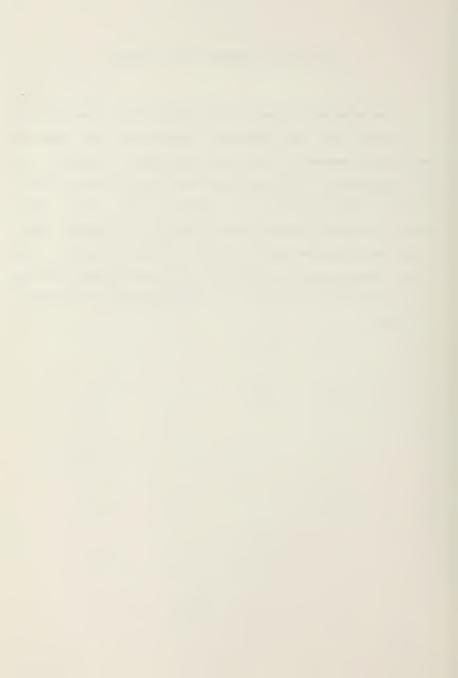
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00222 DIVIDE OVERFLOW - FAULT ENTERED*
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APPENDIX E. SAMPLE TEST PROGRAMS

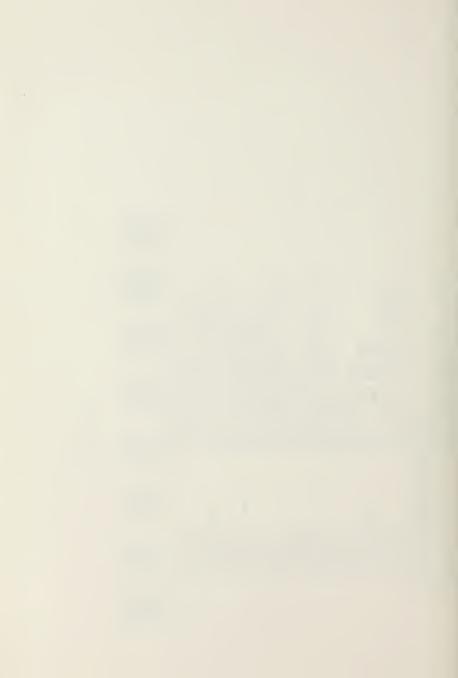
The programs listed in this appendix were designed to illustrate how the AN/UYK-20 emulator can be used for developing programs. The first two programs presented are the generation of prime numbers and the solution of simultaneous linear equations by Cramer's Rule. They depict several AN/UYK-20 control structures such as looping, iteration, and condition code testing as well as numerous load, store, and arithmetic operations. The last program performs the Cramer's Rule algorithm and demonstrates input/output routines.



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                                                                                                                                                                                                                                                                                                LITERAL LOAD, ? INTO REG 11 (CANDIPATE)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            JUMP IF LESS THAN, GET NEXT PRIME CAND.
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  LOAD MULT, PRINES FROM NEMORY INTO REGS
                                                                   00214 NOT IMPLEMENTED-EXECUTION ENDS !
02722 DIVIDE OVERFLON - FALLI TYTERED
52724/401 (1987)
                                                                                                                              LITERAL LOAD, 2 INTO REG 5 (2ND PRIME)
                                                                                                                                                                  LITERAL LOAD, NO. OF PRIMES INTO REG 7
                                                                                                                                                                                                                                                                                                                                                                                            DIVIDE REG, CANDIDATE BY TRIAL DIVISOR
                                                                                                                                               LITERAL LOAD, 2 INTO REG 6 (COUNTER)
                                                                                                                                                                                                                                                                                                                                                                                                                                                  LITERAL ADD, INCREMENT TRIAL DIVISOR
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           LITERAL ADD, INCREMENT PRIME COUNTER
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      JUMP IF LESS THAN, TRY NEW DIVISOR
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      PRIORITY INTERRUPT, HALT EXECUTION
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    . IT LOAD, FORCE FEED 2 INTO REG 01
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          LIT LOAD, FORCE FEED 1 INTO REG 00
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           PRIORITY INTERRUPT, HALT EXECUTION
                                                                                                                                                                                                                                                                                                                    LITERAL ADD, INCREMENT CANDIDATE
                                                                                                                                                                                                                                                                                                                                                        LOAD REG, CANDIDATE INTO RFG 13
                                                                                                                                                                                                                                                                                                                                                                                                                                                                        COMPARE DIVISOR WITH CANDICATE
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                CORPARE, PRIME COUNTER WITH N
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          STORE FOUND PRIME INTO MEMORY
                                                                                                                                                                                                                       COMPARE N (NO. OF FRIMES) & 1
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                                 THIS CARD WILL ENVOKE PAGING
                                                                                                                                                                                                                                                                                                                                                                                                             COMPARE, REMAINDER WITH 0
                                                                                                                                                                                     STORE A 1 INTO ADER 2048
                                                                                                                                                                                                         A 2 INTO ADDR 2049
PRIME NUMBER GENERATOR
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               GO, COMMENCE EXCUTION
                                                                                                                                                                                                                                             LOCAL JUMP, IF FOUAL
                                                                                                                                                                                                                                                                             LOCAL JUMP, IF EQUAL
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                                                       OP236 FAULT INTERRUPT-EXECUTION ENDS .
                                                                                                                                                                                                         ST0 3E
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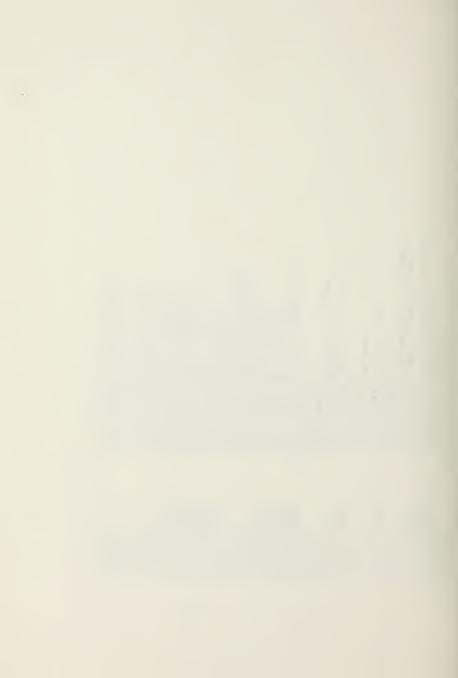
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STORE (RA) INTO Y* AND INDEX BY 1 (STORE SPACES)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                            INITIALIZE BUFFER KORDS COUNT (20 PRT FUFFERS)
                                                                                                                                                                                    RFGISTER CONTAINING TWO BCL SPACE CHARACTERS
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  DECREMENT NEXT COUNTER (NO. OF BUFFERS)
                                                IOCH FOR 20 BUFFERE FROM CARD READER
                                                                                                                                                                                                                                                                                                                                                                                                                                                             INPUT & BUFFERS FROM THE CARD READER
                                                                                 IOCH FOR 6 BUFFERS FROM CARD READER
                                                                                                                                                                                                                                     BOTH EQUATIONS HUST EF IN STD FORM
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                INITIALIZE BUFFER ADDRESS OF INPUT
                                                                                                                                                                                                                                                                                                                                                                                                                            INPUT 14 BUFFERS FROM CARD READER
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               INTIALIZE DESTINATION BUFFFR ADDR
                                                                                                                  DUIPUT 10CW FOP 5 RUFFERS TO PRI
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            INITIALIZE OUTPUT EUFFER ADOR
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  STORE RA INTO Y* AND IMPEX Y*
                                                                                                                                                                                                                                                      A (Y) PLUS B (X) EQUALS C
                                                                                                                                                   OUTPUT 20 PUFFERS TO PRI
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               DECREMENT BUFFER COUNTER
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    BUFFER WORD COUNT
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    DUTPUT 14 BUFFERS 10 PRI
                                                                                                                                                                                                                                                                                                                                                                                                                                         STORE DOUBLE INTO 10CM
                                                                                                                                                                                                                                                                                                                                                                                                          STORE DOUBLE INTO 10CM
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                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     ADD 26 TO EUFFER ACOR
                                                                                                                                                                                                                                                                                                                                                                                           LOAD SRI WITH REG 13
                                                                                                                                                                                                                                                                                                         CONSTANT OF 1ST EQN
                                                                                                                                                                                                                                                                                                                                                          CONSTANT OF 2ND EON
                                                                                                                                                                                                                                                                                                                                                                           LOAD 1 INTO REG. 13
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                                                                                                                                                                                                                                                                                     X COEFF OF 1ST EON
                                                                                                                                                                                                                                                                                                                         Y COEFF OF 2ND EON
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 COUNTER EQUAL ZERO
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     COUNTER EDUAL ZERO
                                                                                                                                                                                                                                                                        COEFF OF 1ST EON
                                                                                                                                                                                                                                                                                                                                          K COEFF OF 2ND EON
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   COUNTER EDUAL ZERO
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  DECREMENT COUNTER
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  SUFFER COUNT
00236 FAULT INTERRUPT-EXECUTION ENDS * 00214 NOT IMPLEMENTED-EXECUTION ENDS *
                              00222 DIVIDE OVERFLOW - FAULT ENTERED*
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    RESET
                                                                             16758
                                                                                                                16735
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NITIALIZE NEXT BUFFER WORD COUNT (5 PRT BUFFERS)
                                                                                                                                                          STORE (RA) INTO Y* AND INDEX BY 1 (STOPE SPACES)
                                                                                                                               INITIALIZE GUFFER ADDR OF SECOND INPUT BUFFER
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        ***CRAMER'S RULE ALGORITHH*** STORE X OF SON 1
***RE-ENTRY POINT FOR REPETITIVE 1XECUTION ***
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  SUBTRACT DOUBLE, RESULT OF DENOM IN OC/01
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       MULT RT. DIAG OF DENOM, RESULT IN 10/11
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             DOUBLE SUBTRACT (EVAL NUM), RESULT 04/05
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   MULT LEFT DIAG OF DENOM, RESULT IN 00/01
                                                                                                                                                                                                                                                                                                                                                                                                                       DECREMENT NEXT COUNTER (NO. OF BUFFERS)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  MULT, RESULT REG 14/15
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    NUM LEFT DIAG MULT, RESULT REG 04/05
                                                  NITIALIZE NEXT OUTPUT BUFFER ADDRESS
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         X NUM LEFT DIAG MULT, RESULT IN CC/01
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 NUM RT. 01AG MULT, RESULT IN 10/11
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 RESTORE CONSTANT OF EGN 1 IN REG C5
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              RESTORE CONSTANT OF EOM 2 IN RFG 15
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      RESTORE X COEFF, ECN 1, INTO REG C3
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  RESTORE Y COEFF, EON 1, INTO RFG C1
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         RESTORE Y COEFF OF ECN 2 IN REG 11
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   X COEFF OF ECN 2 IN REG 13
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              STORE CONSTANT, EON 1, INTO REG 05
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        STORE CONSTANT, EQN 2, INTO REG 15
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  STORE Y COEFF. EON 2, INTO REG 11
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          STORE X COFFF, EON 2, INTO REG 13
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   STORE Y COEFF , EON 1, INTO REG 03
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     JUMP, IF EDUAL (ZERO DETERHINANT)
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        DIVIDE NUM/DENGM, Y RESIDES IN 05
                                                                                                                                                                                                                                    REINITIALIZE BUFFER ADDR IN REG
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            STORE DOUBLE, DENOM INTO 16/17
                          LOAD SRI WITH A 1 FROM REG 13
                                                                                                                                                                                                                                                                                       STORE RA INTO Y* AND INDEX Y*
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        NUM RESULT IN REG 00/01
                                                                                                                                                                                  DECREMENT BUFFER COUNTER
                                                                                                                                                                                                                                                                                                                                                                                            BUFFER WORD COUNT
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          COMPARE DENOM WITH ZERO
                                                                                                                                                                                                                                                                                                                                                                 ADC 26 TO EUFFER APDR
                                                                                                                                                                                                                                                               LOAD AND INDEX BY 1
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       LOAD 00 INTO REG 00
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   RESIDES IN REG 01
                                                                                                                                                                                                             COUNTER EQUAL ZERO
                                                                                                                                                                                                                                                                                                                                                                                                                                           COUNTER EDUAL ZERO
                                                                                                                                                                                                                                                                                                                                         COUNTER EDUAL ZERO
                                                                                                                                                                                                                                                                                                                                                                                                                                                                         LOAD REG 13 WITH 0
                                                                                                                                                                                                                                                                                                              DECREMENT COUNTER
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 LOAD SRI WITH 0
                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      NUM RT. DIAG
                                                                                                        BUFFER COUNT
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                                                                                                                                                                                                                                                                                                                                                                                            RESET
                                                                             01,2,17,00,00330
                                                                                                        01,2,15,00,000035
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                                                     01,2,11,00,08076
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   63,00,15,01
                          03,0,15,05
                                                                                                                                                          15,1,10,11
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BYTE STORE, REG 7 PUST CONTAIN TWICE ACOR
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                                                                                 LOCAL JUMP EQUAL (7ERO QUOTIENT)
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                                                                                                                         LIT SUBTRACT, 1 FROM REG 7
                                                                                                                                                                                                                                                                                       LIT SUBTRACT, 1 FROM REG 7
                                                                                                                                                                                                           LIT DIVIDE, REC 475 BY 10
                                                                                                                                                                                                                                                                     LIT LOAD, C INTO REG 4
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                                                                                                                                                                                     . IT LOAD, C INTO REG 4
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STORE DOUBLE INTO 10CW
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THE INPUT COEFFICIENT VALUES AND CONSTANTS FOR EACH ECUATION MUST BE INSERTED USING LOADER CONTROL CARDS IN THE FOLLOWINS LOCATIONS THE PROGRAM SOLVES TWO SIMJLTANEOUS EQUATIONS BY CRAMER'S RULE.

CONSTANT IN LOCATION 2052 D. A1 IN LOCATION 2050 D. B1 IN LOCATION 2051 D. 2ND EDUATION. 151 EOJATION.

A2 IN LOCATION 2053 0. B2 IN LOCATION 2054 0. CONSTANT IN LOCATION 2055 D.

THE RESULT IS.

HERE, OTHERWISE EXIT REINITIALIZE BUFFER WORD COUNT FOR BUFFER INIT, INSERT LOADER JCL 06 300 0000 TO CHANGE VARIABLES = 0 02053 0 02054 0 02055 6 00031 12

CONSTANT OF 2ND EQUATION
RE-EXECUTE PROGRAM AT ADDR 1055 DECIMAL Y COEFF OF 2ND EQUATION X COEFF OF 2ND EQUATION 00001

TO CHANGE VARIABLES INSERT LOADER JCL HERE, OTHERNISE EXIT NOTIC TOS ON THE RESULT IS.

END EXECUTION

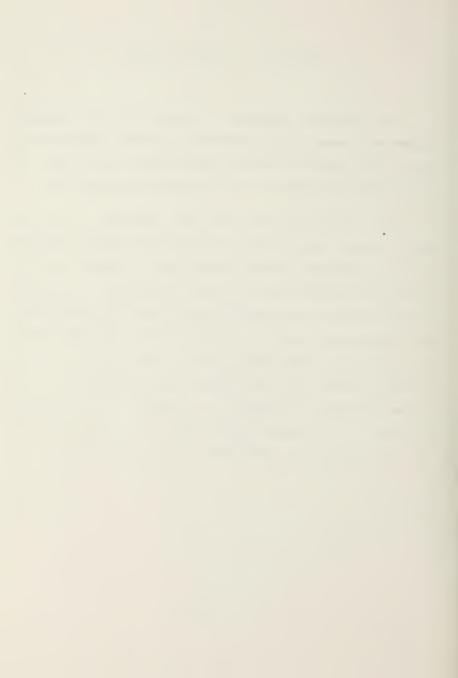
119



APPENDIX F. EMULATOR LISTING

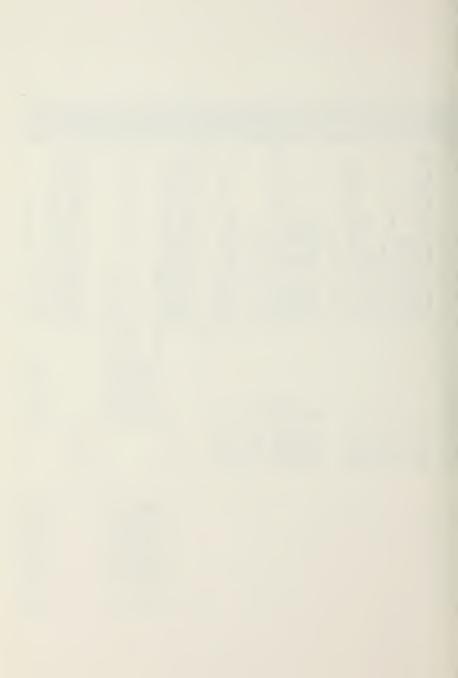
This appendix provides a listing of the TRANSLANG assembler output of the AN/UYK-20 emulation. A source file copy of the emulator exists on disk as well as on cards. A microinstruction object file is also maintained on disk.

The listing is divided into four sections. The left most section contains the microinstruction address composed of four hexadecimal digits followed by a 56-bit microinstruction created from a TRANSLANG instruction. The center section contains the TRANSLANG source which includes labels, an instruction, and/or a comment field. The final number printed on the right most side of the listing is the sequence number of the TRANSLANG source statement. This number, printed in decimal, is created by a Burroughs software utility program called CARD-LIST. This number must be used when editing source programs on disk.

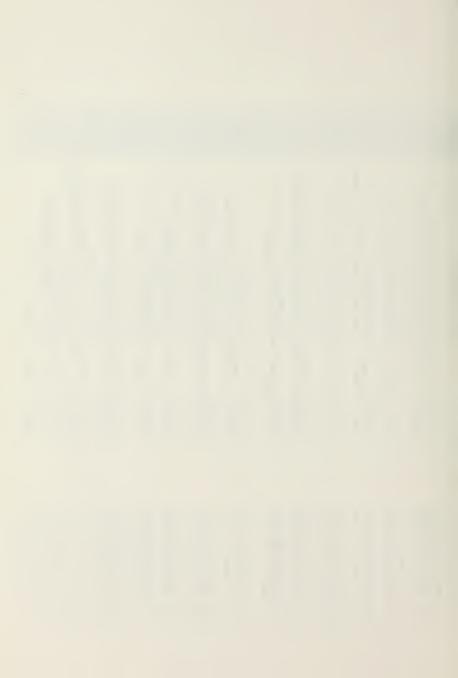


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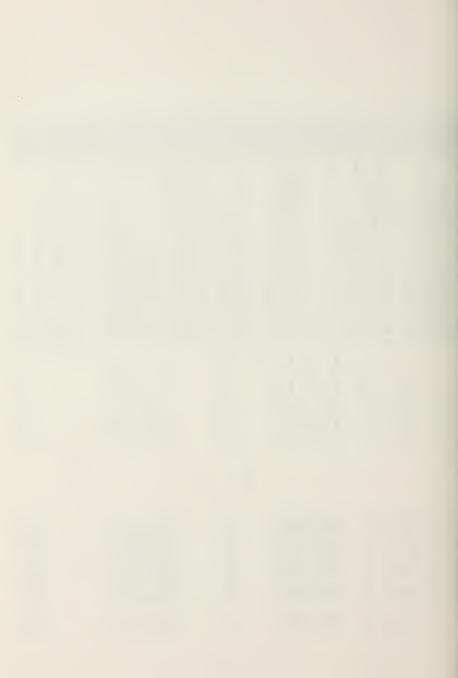
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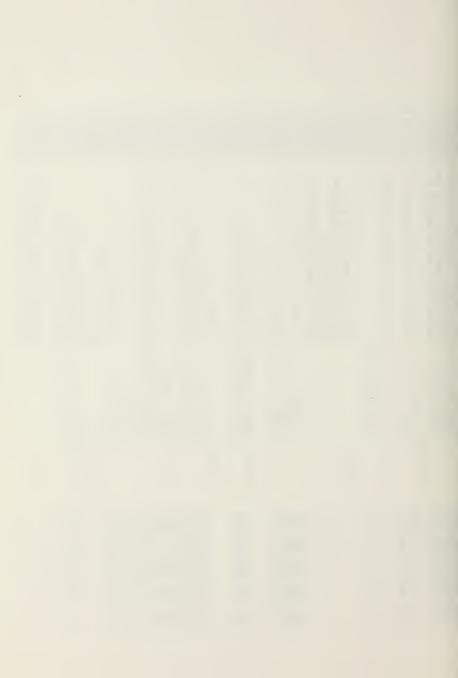
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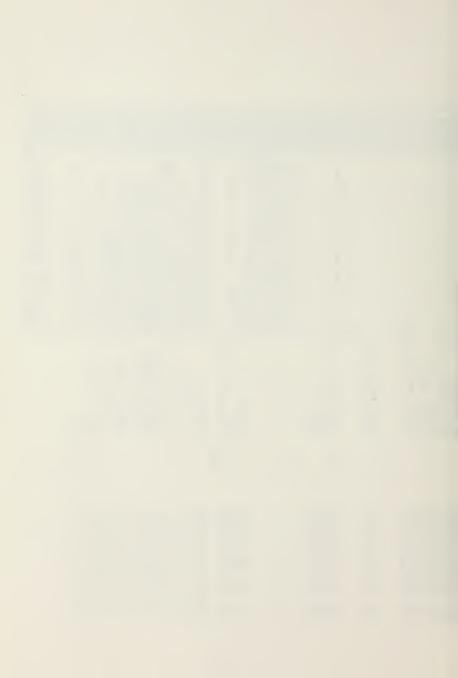
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ARC TO SERVE ARE VOLKER OF THE	WORDS (32 BIT) EACH. THE PACE NO. IN	THE "L" CARD COOL, 5-8) WILL BE	X THE SELECTED PAGE AND STORED IN	THE NEXTINST REG TO BE UTILIZED AS THE	BASE ADDRESS TO LOAD THE PROCRAM.	A ZERU B ARDRESS OF PAGE REFESTER		SET UP CTR FOR 255 + 1 ITERATIONS	THIS LOOP WILL INITIALIZE 256 PAGE ADDROC129CCO	A REGISTERS TO THE MASE ADDRESSES	MIRANCHER DIE 10 FAFTER DESCRIPTING COLSTON	M INTO THE NEXT PAGE ADDRESS	S AND INCREMENT LOOP COUNTER	1 = HAR2; JUHP X INCREMENT APOR OF FAGEOC135C00	X LOAD ADDR OF COL 1-4		€ PEAD COUS 1-4	A DEL UCIAL VALUE UP PAGE NO. 3N CUL.65-0	B = SAR K INTO NXIINSTR REG WHICH WILL	M WRITE THE BASE AGORESS OF SELECTED PAGE 06142000	X TO BE USED AS THE BASE ACORESS TO LOAD OCI43COO	I THE PROGRAM.			X THIS ROUTINE WILL READ THE CONTENT OF X THE HENDRY ADDRESS IN HAR?	K PERFORM READ	READ CONTENTS OF MARZ INTO B.		OC125COO	A AND STATUS DEG 1 CONTENTS AND PACKS		GET ADDRESS IN COL. 5-8 OF "GO" CARD	•	X OFFSET ADDRESS BY 1024	A LOAD ADDRESS OF PSW		STORE COMPLETE PSW INTO HIR AND AL	u	START EMULATION OF UYK2C				KGET ADDRESS FIELD FROM COLUMNS N-M	MOF INPUT CARD. ADERESS WILL BE IN	*DECIMAL. (N & M STAND FOR CARD COLS)	TO MODU SOCK ACMEN SHEET FOR THE SECOND TO SECOND S	A SAVE RETURN		XISOLATE LSB OF CARD(N-3)XW
		× 1		*		AMPER = MARO	AMFCR	254 = LII *	LCTR; SAVE		UMEN SAT THEN B + + = P			IF NOT COV THEN PHAR + 1 = HAR2 1 JUMP				GELADOR - 1 = CPCK	ITT COMP 8		HPCR	•				MR21 IF RDC	WHEN ROC THEN BEXT JUMP					- 1 = CPCR	1 L = A1					- 1 = CPCR	STARTIME - 1 = MPCR X					ar I		2	0F = A2	SAR	148=L17
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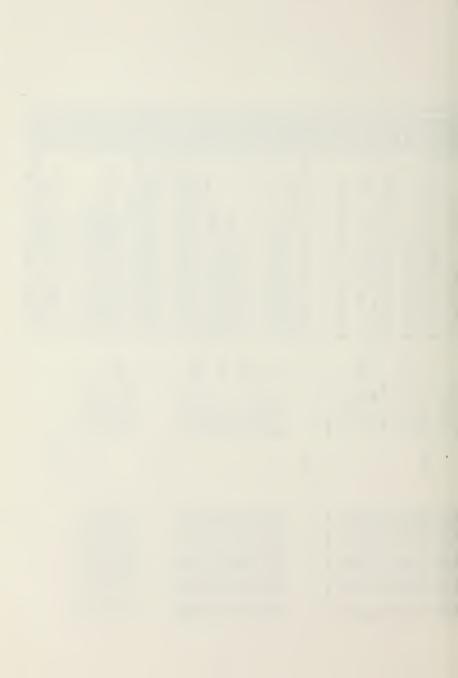
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NAK ALOR FIELC F. IN B. RAKK ALOR TREAT AS O C. IN B. REG HUMBERS INTO SINGLE VORD SECTIAL NUMBERS INTO OCTAL	X NEEDED FOR AMPCR ASSIGN FRIDK TO JUHF X I HIS ROUTINE PERFORMS A PEHORY WRITE	10P 10 READ NEXT CARE THEN 10 CONTROL SEXCE CARE NOTINE. OF AND CARBUFFER ES FOR ECHO PRINT BOUTINE. ES FOR ECHO PRINT BOUTINE. OPDS VILL HAVE SPACES	EHORY ELSE SKIP	* RETRIEVE CARD ** CARDVUFF ADDRESS INTO B SKIP ** IRC INCICATES CAT INPUT ** CONTENTS FOR MAILBOX SKIP ** IRC -> FALCE THEN CHO PRT (PTK) ** JUHP TO CONTROL CARD ROUTINE	KATIR CONTAINS 1/HEXADDR X X X X X ECHO CARD READ CPCR X JUHP TO EXIOF ROUTINE 1 = HPCR X JUHP TO CONTFOL CARD ROUTINE 1 = HPCR X JUHP TO CONTFOL CARD ROUTINE	X THIS KOUTINE PERFORMS THE 10P INTERFACE AND PASSING TO THE FUNCTION
N = A1 1 ECL LIT 1 FUL THEN 0 = B1 ST LLBLANKS - 1 = FPCR ACKED-1 = CPCR ECOCT-1 = CPCR	Z = AMPCR UNP UNP	0 = EC6ALCIR 1 = LIT = LIT = LIT COMP 16 LIT = MAR?	JIPUII - 1 = CPCR F NOT COV THEN EMAR PACES-1 = MPCR	ARON SECTION OF SECTIO	P 16 = SAR HIR 0P - 1 = CP 0PRINICO - 1ROLCO - 1	
	ALLELL BL.	NEWCARD:	SPACES:	CARDFE ICH: C C C C C C C C C C C C C C C C C C C	CON B = B ECHOPRINTCD: EXT CON	EXTOP:
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	MIN THE B REGISTER.	0						SET GC2									CRT READ CODE FOR CARDFFICH ROUTINE						NORD IN UNPACKED DECIMAL FORMER DIGIT	DECIMAL NUMBER). THE NUMBER IS PASSED	IN A1. THE FACKED DECIMAL EDUIVALENT	OF THE NUMBER IS RETURNED IN B REGISTEROC26600	WHICH CONSISTS OF AN 8 DIGIT DECIMAL NOCC267C00	THIS SIEP IS UNITITED FOR A 4 DIGIT RC.	LERU MIN TO OCCUPANT LOSD IN TIMES	SEL COONIER TO FIRE CONT. 4 111ES		% ELIMINATE HIGH ORDER 4 BITS OF MSB CHARGO273C00	SHIFT AL RIGHT 28 BITS AND "OR" WITH	K HIR AND PLACE IN 3 REGISTER K LECTHOSI DIGIT NOV IN HIGH DROFE	A POSITION OF MIR.	= A11 STEP FLSE SKIP # SHIFT NEXT DIGIT	% INTO POS. FOR NEXT PASS THROUGH LOOP %BRANCH TO TOP OF LOUP	A CHECK TO SEF IF AN 8 DIGIT NUMBER	% JUMP TO THE END OF THE REUTINE # 15 ONLY A 4 DIGIT NIMBER WAS INPUT.	PREPARE MAR TO READ NEXT 4 DIGITS	# B NOW CONTAINS LOW ORDER 4 DIGITS		WHEN READ COMPLETE, SET AT EQUAL TO B	BRANCH TO THE TOP OF THE LOOP	ARETURN TO CALLING ROUTINE WITH PACKED	KNUMBER IN B REGISTER		THIS ROUTINE WILL CONVERT DECIMAL	NUMBERS INTO THEIR OCTAL EQUIVALENTS.	A NUMBER PASSED VIA THE D REGISTER. THE
8		SET GC2 WHEN GC2 THEN NOT	SAI	WHEN SAI THEN OF SET INT	IF INT	WHEN INT THEN STEP	BEX # HR2 # IF RDC	WHEN ROC THEN NOT BY RESET	# 15 13 1100 NJW 100 11		t	MW21 IF SAI	WHEN SAI THEN DI JUMP	*	*		A2		A2 OR B = B			*	*	×	~	×	94	SEL LCI	***	T = 11Tr COMP u = SAR		L = A1		SNI C		IF NOT COV THEN ALL =	PACKTOP - 1 = MPCR XE	SKIP	PACKEND - 1 = MPCR &	BHAR + 1 = HAR2 %I	c		WHEN RDC THEN B = A1 8	NEXT4 - 1 = NPCR X	JUHP KI			· W	at s	* 🗷
											OUTPUTE						CRIINS					PACKED								+ F Y L	PACKTOP													PACKENDS				DECOCT		
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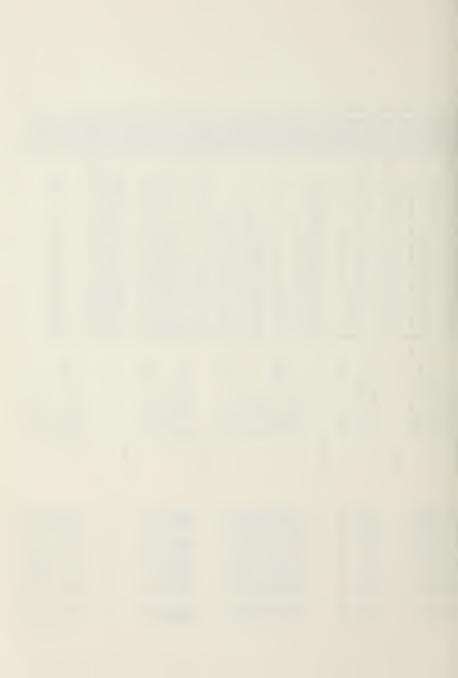
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DOTAL EQUIVALENT WILL RE RETURNED IN B.OC.290COD PACKED REGULIS ARRIVE IN B RFG 002394COD CLEAR B REGISTER 0730COO SET COUNTER FOR 7 ITERATIONS, 00301COO	TO THE PECHAL NUMBER 111 A1 AND CLEAR B-0020200 1 OF PUT HIGH ORDER 4 B11S OF A1 11N10 1 ON CROKE 4 B11S OF A3. 1 ON CROKE 4 B11S OF A1. 1 ON CROKE 4 B11S OF A1. 1 ON CROKE 4 B11S OF A3. 1 ON CROKE 5 B11S OF A1. 1 ON CR	X CONVERT DECHAL DATA IN COL 13-20 INTO X COLAL AND STORE AT THE ADDRESS IN X COL 4-8 X RETRIEVE ADDR IN COL 4-8 IN OCTAL X RANSER ADLOP TO A3 FG X LOAD ADDRESS OF COL 13-14	P SARD	THIS ROUTHER VILL INSERT DATA INTO THE CC39000 REGG. THE DATA TO BE WRITTEN IS IN HIR-OCC492000 REGG. THE DATA TO BE WRITTEN IS IN HIR-OCC492000 REGG. THE DATA TO BE WRITTEN IS IN HIR-OCC492000 REAC CONTENTS OF NATINSTE OCC494000 REAC CONTENTS OF NATINSTE OCC494000 REGG. DATA AT THAT ADDRESS (CHR.2) OCC394000 REGG. AND GET THE NEXT CARD OCC494000 WRITT NEX ADDRESS WRITHSTE OCC494000 WRITT NEX ADDRESS WRITT NEX AD
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S STORED IN THE DESTRED GENERAL REGISTER. 00359000	K ISOLATE COLUFN 2		K B IS NOW OCCEN REG. NO. 13 OR 1 (NO. 23	ERAL REGISTER STACK	S HULTIPLY BY 16			A LUAD ADDR OF CARF COL 5-P		A READ CALO DES	A ISOLATE CARD COL /-8			A DOUGH TO CHO LINE IN ROUTING (4 UTGIT NO.)	A DIAS UCIAL VALUE OF GEN REG NUMBER	* HOVE DAKE ADDR TO AS FOOM DOS		% CREATE GEN REG ADDR (BASE + OFFSET)		K ADDRESS OF DATA	M READ IN DATA		A SET MARI AS MOST RECENTLY REFERENCED	A LUAD GEN REG AUDH INIU HARZ	SHIFT TO ISOLATE BRI	R H HAS UCIAL VALUE OF DATA	SOPECIFIED GENERAL REGISTER		r set	RSET UP BREAKPOINT REGISTER AND SET	& STATUS BITS	S FILL B WITH CARE COL 1-4 (FROM SWI)	R ISOLATE THE ROWAG CHARACTER		RISOLATE COLUMN 2		WRITE PSW INTO B		A INPUT FROM HEMONY	ACHECA FUR CHARACIPE IRI	LITI SKIP		_		& JUHP TO PREAKPOINT WRITE SUBFUNCTION		•		THIS ROUTINE	M REGISTER AND SETS THE READ STATUS BITS		000 000 00 00 0 100 100 0	S WRITE PSW INTO MEMORY	
	0 to 1 to 1	COTT 0 % 0 XX	- 1 ×	8 L = 8	COMP 4 = SAR	B L = BRISLMAR	COMP 8 = SAR	CIT # HARZ	CARDSX8 = LII	intol 1 a crea	8 T 8 B	CURP 16 = 5AR	0.000 - 0.000	STORY TO STORY		0 0410	2 2 3 3 11 2 2	A1 + B L = BR1	COHP 8 = SARJ CARO13X16	LIT = MAR2	INPUT - 1 = CPCR	GETAGOR - 1 = CPCR	ASR	BUAN K = MAK2	21 (V ¥ V)	B = FIR	4			BREAKPOINT:		BEX	B L = A1		A1 R = A1	24 = SAR	LII = HAR2	I I I I I I I I I I I I I I I I I I I	INPO = 1 = CPCK	41 = LI		DRKREAD - 1 = HPCR	54 = LIT	IF FALSE THEN SKIP	BRKWRITE - 1 = MPCR	BAK BOTH -1 = MPCR			BRKREA0:		1 L = AI	0 1 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	1 1	
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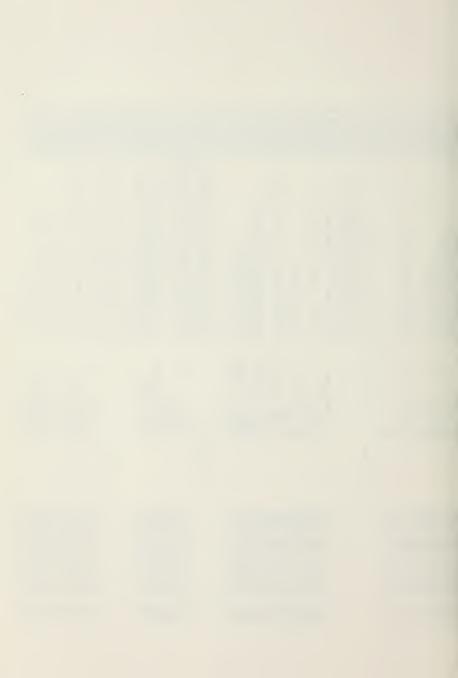
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JUMP		REG 15		MSET BIT 21 OF PSW REG	X WRITE PSW INTO HEMORY	JUHP	# THIS ROUTINE SETS UP THE BREAKPOINT	REGISTER AND SELS II		X SET UP AT WITH MASK BIT POS. 21/20	P U I	21 AND 20			ATHIS ROUTINE WRITES THE DECIMAL ADDR	INIO INIO REGISTER RET	RETRIEVE CARDIX4 CONTENTS		INPUT INTO B		GET ADDRESS OF	A P HAS BINARY ADDRESS VALUE	NOF	WRIT	RETURN TO NEW CAED ROUTINE			MHANDLES SECOND WORD OF IND WORD INSIN		SRELDAD ADER OF CARD COL 13-16	ROMIT PEX STEP IN GETADOR, B CONTAINS	COL 16 DIGIT IN LSB OF B	*LOAD OCTAL VALUE OF DATA INTO SECUND			THIS ROUTINE WILL PACK AN INSTRUCTION	INPUT CARD INTO A 16 BIT INSTRUCTION AND PLACE IT IN THE LS 16 BITS OF A	32 B	ARE	ROUT		RFAD	ISOLATE 11 BITS (CHARACTER + 3 BITS)	ISOLATE NEXT OCTAL DIGIT			
pt.	SC (× ×		S	ыt	w w	94			111		w 1		we	× 1	× ×			W W			pe 1	-		×	×	× i	× ×	= [11	*	8.0	. .	¥ >		*		SC SC			w		SAR		art			
MPCR					œ	WRITEBRKPT - 1 = MPCR & JUMP TO WRITE BREAKPOINT RFGISTER S				to		9							a					~	œ					ì			= CPCR	:								н					
1 =					CPC	n				9 75		9	5						CPCR = CPCR					CPC	MPCR				013)		œ		MPCR									# 21 PCR					
1				SAR	- 1 = CPCR	ı -			-	= SAR, 48	= MIR		7				2	CARDIX4 = LIT	INPUT - 1 = CPCR		_		0 4 0	0JIPUI1 - 1 =	#				16 = SAR; CARD13X16	2	GETADOR = CPCR	•		•							2	CARD5X8 = LIT; 2 INPUT - 1 = CPCR	,		SAR		
BRKP			= A1	21 = B =	- 11	B R K P			= A 1			;	1				= MAR2	# # X	1 90	HAR	= 1	2	B = B	, <u>,</u>	RO -			11	SAR	MAR	DR =	2	NSTR PD -	2							HAR	8 1 8 1	A 2	A 3	13	SAR	
WRITEBRKPT			1 1 =	COMP 21 = A1 OR B =	OUTPUTI	=			= 1 [1]	COMP 16	P 0R A1						n 	IR D1	TAUT	LII = MAR2	BKPT = LIT	B = MIR	COMP A = CAD	11 PU	MCA				: 11	LIT = MAR2	TAD	= A2	LOADINSTR NEWCARD =			=					LIT = MAR2	AP UT	B R = A2	B L = A3	COMP 13 =	c 11	
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		BKKWKITE					BRKBOTHI								WRITEBRKPI													DOUDLEWORD:								INSTRUCTIONS											
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0216				3000 0		022C 0			4809				1190				4809 2		0460			4809							0700				0236									9780			2000		
COF2			OOF3	OCF5	0 C F 6	0 f F 7			0 0 F 8	CCF9	OCFA	-	9111				OFF	DOFE	OCFE	C 1 00	c 1 0 1	0102	0103	0105	0106			0107	0108	C109	010A	0100	0100								C 1 0E	0106	0111	0112	0113	0115	



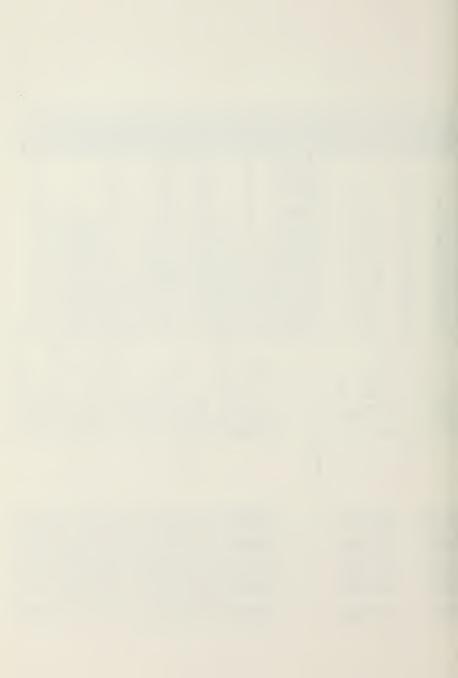
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R SET UP A Y-SELECT	IN A2 AND SHIFT 2 BITS FOR NEXT FIELD	R ISOLATE FUNCTION BITS	2 * LIT		K PACK FUNCTION BILS (0-3) INTO A2		K READ IN NEXT 4 COL. (9-12)		A ISULATE COL. 12 TO CHECK FOR COMMA		COUR FUN COMMA	s or privat a the Al Col. 10-12 AS "C" FIELD	A TOAMSTO WO DETWOOD DOLLTON	A CANDER TO RELITED TOURS THE D	A CARU HAS CUL. IU-II AS "A" FIELD	A COL. 13-14 AS -11 - 11-15		# 150LATE 1 PIT OF CC 10 + 3 BITS			R ISOLATE CC 11 (381TS) INTO B		% INSERT "A" FIELD INTO AMFCR		= [[]]	c 1 A		KISOLATE BIT WHICH IS COL 13 DIGIT(1,0)		FFILL A1 WITH FIT-0-0-0 (LEB)		APUI COLIU IN ESB OF ASSB	KPUT COLLU IN ISB OF B		R COMBINE COL. 13 AND 14	K FINISH BUILDING 15 BIT INSTR	A LOAD INSTRUCTION (AS UNCHANGED)	R A3 CONTAINS COLS. 15-16 IN UPPER HALF	\$ SET UP COL 15 IN LSB OF At		KCHECK FOR COMMA(s)		XCOLS. 16-2- OF CARD CONTAIN DECIMAL	8 :Y: FIELD	S GET NEW CARD			MINISTRUCTION WILL LOAD AN ENVIRONTION WINNERS IN AV	S-KEHORY WO	A1 IS A TEMP RETURN ADDRESS REG		PEAD	S SAVE NXTINSTR IN CTR (COPPLEHENTED)
A2 = AHPCR A3 + AHPCR L = AHPCR	2 = SAR	B L = A3, CSAR	COMP 30 = SAR # CARD9X12		= A2		INPUT - 1 = CPCR	۸1		A1 EUL LII		IF FALSE THEN STEP ELSE		MILITER 1 - UTCH			COMP 15 = SAR		28 = SAR		- 111		B = AMPCR	A2 L = A2	A A A A A A A A A A A A A A A A A A A	117 - MARD	14PUI - 1 = CPCR		P 7 = SAR	A1 R = A1	28 = SAR	81					- 1 = CPCR	A3 L = A3	V V V V V V V V V V	58 = LIT		N STEP ELSE	DOUBLEWORD - 1 = MPCR		MENCARD - 1 = MPCR			LUAUINSIKE				NSTR = LIT	LCIR
00F0	0030						0900		0000			0 40 3		0 7 0		0 20 0			0030		0040			0000				C 0 F 0			0030							0101					0000		2620								0 40 0
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	MAR2		RE IN AZ TO MIR	FHORY	WRITE LOAD ADDRESS		S MEHORY URITE	TURN ADDRESS	R REGUIRED BEFORE JUMP 01	Ö	~ 1	A TURE DOUTTING UTIL DISCOLUTE A		THE	100				S CC COL. 2 INTO LS BYTE OF B		% MASK OFF COL. 2		X CHECK FOR M1	All SKIP & SET BIT 30 OF SRUZ FOR CRI	K READ IN CONTENTS OF SRES INTO B			VIENTS		20		1	A NORBER OF MEMORY CELLS AS INDICATED BY CO	S GET NUMBER OF CELLS AND CONVERT TO DOTAGE	A A1 CONTAINS NUMBER OF CELLS BEING SAVEDONS77COC	00		TENTS	* NEXT INSTRUCTION AGON TO BIK			20	D INTE	10-12)	# COL 10 TO LS 3 BITS OF AZ	NO EA 30 021 OTHE STIRE & A 01 102 STAINST P	2	X COL 11 TO LSP OF A1 OC			1 A3 = COLS, 10,11, + 3 BLANKS OC	X ISOLATE COL. 12	
INPUT - 1 " CPCR		P + 1 = P		OUTPUT1 - 1 = CPCR	NOT CTR R = HAR2	HAS B PS	OUTPUT1 ~ 1 = CPCR	CR	STEP	JUMP		TAT DE LATE					III = MAR2, BFY	STATUS = 131	8 2 8	16 = SAR1 63 = LIT	L11 AND B = A2	1 = SAR		IF IRUE THEN BIOC C =				OUMPREG - 1 = CPCR	NEWCARD - 1 = MPCR			RESERVESPACE 1		GETAGOR - 1 = CPCR		LIT = MAR2	NXTINSTR = LIT	INPUT - 1 = CPCR	AI + B H IIK	4			RITYPE1:		B R = A3	16 = SAK) / = LII	COMP 3 = SAR	B R = A1	8 = SAR	A1 AND LIT = AMPCR	AS OR AMPCR L = AS	LIT AND B = B	
0900 3000 0000 3960	0043 0010	0636	0600 0000	0000 0000	CB0 2 841C	0000 0000	0810 0000 0000 0000	APC 3 00 1C	0000 0000	4820 0003 0010 00F0							HANG 2003 OCTE ONED	0000 0000	0000 0000		2055 2030	0000 0000	C00 2 0030	1409 0000 4000 00F0	0000 0000	ACS C080	0000 0000	0260 0000 0000 0060	0600 0000 0000 0090					0510 0003 0030 0060	0004 0000	2003 0010	0000 0000	0900 0000 0000 0900	000					0			0000 0000	0000 0000	0000 0000	A155 0040	4809 E653 1030 00F0	2056 0030	
0149	0 1 4 A	0148	0.140	0140	0146	0146	0151	0152	0153	0154							7 7 7 7	6156	C157	C158	0159	C15A	0158	0150	0156	0156	0160	n161	0162					0163	C164	0165	0166	0167	0110						C16A	0168	0160	016E	016F	0170	0171	0173	



0 9	ے	0		_	٥	2		_	_	_		_	ے	6		٥		_	0	0	٠,	_	_	٠.	٥	_		_	ے		_	٥	٥		٠		_		_		_	٥		_	2	_		_		_	_	_		_	_			_	٥		5	_	_	_	۵.		_	_	٠.	_	_		2	_		_	_		_	_		_	_	_		0	
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					PI ETEO				186 921								10									ARACTER	CIDING CIADITING IN CO. O HILL FINDINGS	IL FIRDIN	THEN BE	The sound of the sounds of the orders		COL. 4-8 IS PLANK, THE STORAGE ADDRESS	 WILL DEFAULT TO THE ADDRESS IN NXTINSTROC623(00							CONTRACTOR AND TO GOOD SHARE OF COMME	STRUCTION								MINTO	0 1 2	IN MAR2					311		E ANALIZEURCESSCOU									SE LU1	T ADD VALUE TO (*) SO THAT SPACE AFPEARS															CHECK IF YOU ARE AT THE UND OF THE CARDOC655CCC				
1 5	ON CF B		INTO A2	200	PE 1 COM				HE PAG	PSW				AU		B 1	SELECTE	110110		MID						O THE CH.	TALL O		ING WILL	100	IN COL.	IE STORAG	 008655					0	0	MA ANDRE	NE N			SS FIFI			01.010	NO. 1	C NOTTE	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0L . 9-12			0 C K		TECATION		0 8 10 6		DACTED	111111111111111111111111111111111111111						SINING SE	HAT SPACE			TIMES		F 2 3	DRESS	2	METONY	55	C retition	O P DO P			ADJURE SE	HE END DI				
0L - 10, 11	OR ADDITE		DITS		LORO RITY				WILL SET	POS. 22) OF THE PSW				FNTC OF F		811 10 LS	FICPACING			FOU INTO						VILL REA	INC IN CO	22 21 22	THE STR	S ADDOLOS	E AUURESS	PLANK, TF	 10 THE A	1000	ION EITS			1 000 M	IN COL.	2000	S AUUR UF			ANK ADDRE				OF NAI	A DO T O C	0 0 000	ADDR OF C			4 CHARACIER BLOCK		COUNTED COD II TIECATIONS		ACIER IN		THOCT CUA	ייים וכחיי	HASK			CF)	4114	י אור או	1 05 (*)			F DONE 4		FEAU AUUR	WRITE AD	100	BLOCK 10	11F ADDRE	47 (8) 21	1			HAVE READ	ARE AT T				
0= 0000/00-00L, 10,11,12	PARE AZ F		K REMAINING		INSTRUCTION LORD RITYPE 1 COMPLETED				SRUULINE	1 POS. 22				DCAD IN CONTENTS OF DCU		MOVE PAGING BIT IO LS BIT	PAGING BIT SETUPACING SELECTED			CONTENTS OF FSW INTO MID						THIS ROUTINE WILL READ THE CHARACTER	TALC CTADI	2000	A DUDTE ("). THE STRING WILL THEN BE	Dro AT Tu		. 4-8 IS	 L DEFAULT		CLEAR CONDITION EITS			4000500	GEL AUDICES IN COL. 4-8	CONTAIN C	C CONTAIN			CHECK FOR BLANK ANDRESS FIFTIN		STEP ELSE EKIP	OCAL DO STUTE OF WATERDER	CONTENT	PONTATME	2014 1000	SET UP READ ADDR OF COL. 9-12 IN MARS			KEAU A 4 CHA		di		L CHAR		EVIDACT CICUTHACT CHADACTED	1011	SET UP 6 BIT HASK			R TEST FOR " (CF)		A IF A (") IS IN THE	VALUE TO		BARIES SEL LIS	S CHECK IF LOOF DONE 4 TIME		OF NEAL	MAR? NOW HAS WRITE ADDRESS		WRITE 4 CHAR BLOCK TO MERONY	INCREMENT WRITE ADDRESS	OND 2 2 2 20 20 2	7 CHECK			A3 AND HA42	CK IF YOU				
# 0 = 0			% PACK							118) %				A D C A		AOH	R PAG			S CON			•			S THI			8 A 0	013 8		A COL	- X		, C.E.					0414				S CHE					. 4		300			* KEA		100									S LES			Z ADD	0	2 1 1 6 9	S CHE		30 00	S HAR		N M H	RINC		ELSE SAIF	MPCD		N A St	* CHE			E SKIP	
					= CPCR	~							≈ SAR	Pro			•																					0000 -				_				SET LC21	0.00	2				_		= CPCK				2		,	,						25 11		0 . 11		EN JUHP				0000	CPCR		2012 0212	ı	-						SIFF ELS	
H 6		~			-	Š							22	٠	1	A.R	-00				0.004																					-				2	6	٠				-		-		0 >		N N		- 4.2						14	2		-	_	I		2		-	"		ú	n	č				-	٠.	_	
8	= A2	8 = SAF	B = A2	O A O A	NSIR -	= 1					004	2 4 4 1	_	T t = CPC		8 CS	O B O	,	_	1 B	1	1															~	00	UK - 1	MADO	JAK L	SIR		0		UE THE		1			HAR2	X 12		5	_	V		e e	A R	O O I	2 .	_	111			Test	00 111	11	4 THE	I HEN	T COV I		V : T +	MAR2	,	1 - 1	1 = A1	4 7050	1 1150	APSTRI		MARZ	0 111	7 V B V	700	UE THE	
A3 OR B	A2 L = A2	COMP 8 = SAR	A2 + B = A2	Oxon or o		001 - 1 = MPCR			202		COAM - VY	2 11 - 117	PSW = LIII 22 =	I NP 11 T 1		B C = B, CSAR			1 = [B H IR		1				RING:									IF LC1		11 11	CETADOD - +	SELAUUK - 1	ITT - MADO	C11 - UAR2	NXTINSTR = LII		8 501 0		IF TRUE THEN SET LC2;	TUBIT . 4 - COCD	1 - 10 - 1	B = A1		LII = MAR2	CARD9X12 = 11T			3 = [1]	I CTD: CAVE			B = SAR	- G ONA TIL	010	63 = LII	A2 501 11T	20 50 50	15= LIT	TO THE THE PART OF	IF IRUE INC	33 = 1.11	10 . 0 4 THEN	IF LUI IMEN	IF NOT COV THEN JUMP		GRAK + 1 = A	A1 = MAR2	***************************************	001F011 - 1 = CFCR	A1 + 1 = A1	104 105	IL LLI INEN	FNDCHARSTRING		A3 = MARZ	A3 LEO LIT	T11 - 28X770073	- 101/101	IF TRUE THEN STFP ELSE SKIP	
8	AZ L = AZ	COMP 8 = SAF	A2 + B = A2	Ox ON CO TO					SELFAGINGS		COAM - TT	2 uvii = 117	1 = MSA	INPIT - 1 =		SO 48 = O B	O B B C		1 = []	P = MIR		1				CHARSTRING:									IF LC1		11 LL2	PETADOD - 4	SELAUUK - 1	COAM - TI	7 HAR - 117	NXTINSIR =		8 501 0		IF TRUE THE	TUPIT - 4 -	1 - 10 - N	B = A1		LII = MAR2	CARDOX12		HORECHAR: INPUI	3 = [1]	I CTD: CA		19 = 7 p		D OWA TIL	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	63 = 111	A2 ED1 11T	על בסוג ווו	15= LIT	107 710	IF IRUE IME	33 = 111	THE POST AND	IF LUI INEN	IF NOT COV I		WILL + I II Y	A1 = MAR2	1 12110 4110	0.0112011 - 1	A1 + 1 = A1	2007 400 20	IL LLI INEN	FNDCHARSTRI		A3 = MARZ	A3 LE0 LIT	- 7874 COOL	- Joy//Our	1F TRUE THE!	
A3 0R B	AZ L	COMP	A2 +		0407	100			SELFAGINGS		* * * *		25.0	I GN I		3 8	J R GO III		***	G.	100	- T - 100				CHARSTRING																											0411011011	TORE CHAR:					II 60															Α1													
00FC A3 0R B	00F0	0030 COMP	2000 00F0 A2 + B = A2		CCCC LUAU	100			SELFAGING		COAL - 111 - 11100		00A0	114P1		8830 40F0 B C = B, CS	O B B C		COE0 1 =	00.90 COFO		1 1 100				CHARSTRING								4 1 4 4		0.00	0.100	+ - 0004 133	0000	0000 0000	0.400	0000 0000 0000 0000 0000 0000 0000		0000		DOTO COFO	THE THE PARTY OF T	0000	10.30 FOFO		001C CCF0 LII = MAR2	CARROTT CARROTTS	0.00	UUDU HOKECHAKI	0000 00Ec 3 = [1]	ON 1 DOE O LETP SA	0 100	0.400				0300	0000 0000 A2 501 11T		0.00 0.0E0 15= LIT	217 71107 71	0.00	0000 0000	0 100	0.00	0C3C COFO 1F NOT COV T	6 1 6 6	0.10	COIC DOFC A1 = MAR2	0.00	0900	4C30 COFC A1 + 1 = A1		0.100	DOOD DOG PROCHARSTRE		0.010	0070 00F0 A3 LEO LIT	- 487640040	000	0000 OOFC IF TRUE THEM	
080C 00FC AS 0R 8	2500 00F0	0000 0000 COH	00F0 A2 +	0,000	0000 6666	100			SELFAGING		7.1.	200 0100	0000 0000 PSM	I GN I		40F0	0.0FC . 117 DP B C		***	COFO E		- T - 100				CHARSTRING:									0 10 0	0 100	0.00.00	0700	0000 0000	0000	0.400 0.100	0 3 0 0				0400 0500	0700	0000 0000	40.00 POF 0		CCFO	0050	0,000	UCJU DOBU TORECHARS	0 E C	00011 0050	0.00	0.100 25.00	0000 0010	9300		003c 00E0	0000		0 3 0 0	0 200	0.00 00.00	0000 0000	0000 0000	חווזר כחות	0 0 0 0	0100	10.30 C. OL O	0.0FC A1	0,00	0900 0000	4C30 00FC	0000	0.00 00.00	0040		0.000 0.000	0010	0000	000000000000000000000000000000000000000	00FC	
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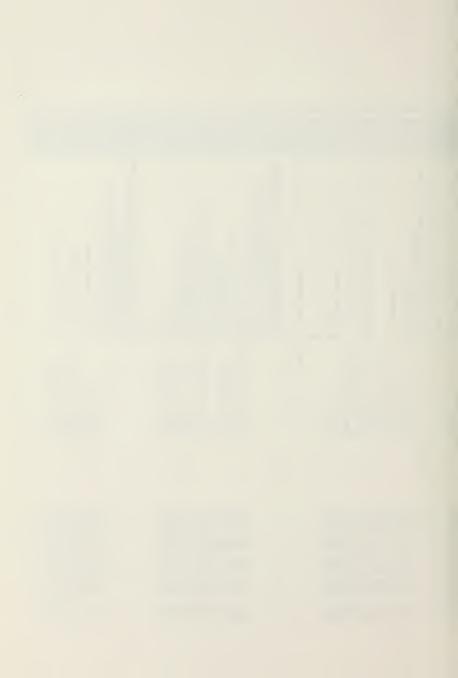
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STEP (LSE SKIP	S STORE AL CONTENTS INTO MIR	X LOAD MAR? WITH ADDR OF NXTINSTR	UPDATE CONTENTS OF MXTINSTR					SWITCHES 1 AND 2. MAR? CONTAINS ADDR 00669C00						I REREAD COL. 1-4 INTO B	COL. 2 INTO LS BYTE OF A1					% READ INTO B THE CONTENTS OF THE FSW			SKIP		SET COL 29(DIFAULIS TO SNAZ BEING SET)	110 115	# DECTION D				X SET BIT 30	RESTORE P VALUE IN MIR				A THIS ROUTINE SETS THE 2 AS BITS IN SPUZOC698000	A FOR DUMP REGISTER CALLS TO CKT UK PIK	TOOLST A THIN OF THE POST OF T	A CONTAINS COL 2 OF CONTROL CARD		# 15 COL. 2 A 17	A11 SKIP	PRINTER MASK	SQUZ INTO B	I SET MSB OF SR # 2				AN/UYK-20 EMULATOR * * * * * * * * * * *		T T T T T T T T T T T T T T T T T T T		
FNOCHARSRING IF NOT COTHER SIFE ELSE SKIP NOT A NOT CARD	A1 # HIR K		OUT - 1 × MPCR ×		*	SWITCHES			~	•	~	~	*	INPUT - 1 = CPCR K	B R = A1 K	16 = SAR1 63 = LII	A1	LIT = MAR2 K	PSW = LIT	r CPCR	=	1 = 111	IF TRUE THEN STEP ELSE	SEFCOL30 - 1 = MPCR K	E C R By CSAF				SETCOL30: B C = P, CSAR	30 = SARJ 1 = LIT	8 11	= MIR	OUT - 1 = MPCR	e i		×	STATUSZ = LII X		10 = 3AR) 63 = L1 A			IF TRUE THEN BIO1 C = A		INPUT - 1 = CPCR R		OUT - 1 = MPCR	×		N T T T T T T T T T T T T T T T T T T T	* 1			; et
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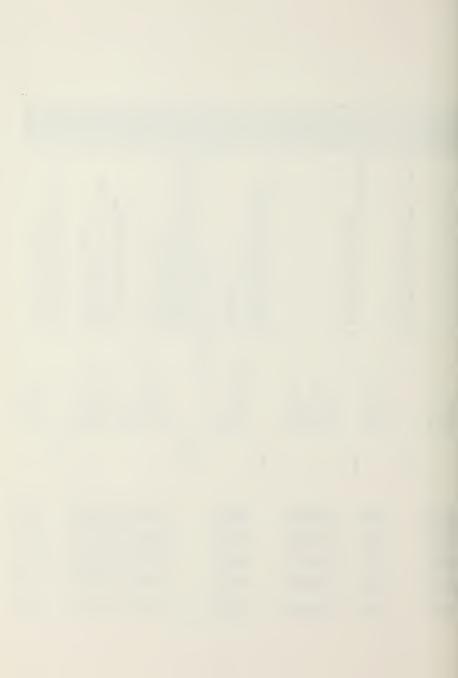
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	ROUTINE TESTS IF THE	S THE 181 FIELD. IF EQUAL LC2	= RA				A CONTAINS "A" FIELD	AZ CUNIAINS "A" FIELD					E W I	TEST FOR WRAPAROUND AND CALL OPCODE	PAR ISOLATED IN 1HW OF AZ	HE C	K CHECK FOR WRAPAROUND	AT FLSE SKIP & PACREMENT PAR	S CALL OP CODE FOR NEXT INSTRUCTION	AR					SET FAR TO 1024	INSI			THIS INSTRUCTION TEST THE LSB OF	SVI	OR (RCH+1)) AND DIVIDES E BY	P CONTAINS RESULT	LCZ = I IMPLIES IS BILE	2	R TE ISB OF B	102	A B DIVIDED BY TWO			*		SKIP & THIS ROUTINE WILL SET THE	IS SEL UPUR EFTR			ROUTINE CLEARS THE CARRY BIT	(POSITION 28) IN PSW							THIS KOUTINE SETS THE CARRE BIT
	UTIN	THE	1 3				SNI	2					UTIN	RW	LATE	I III	W 20	SKIP	CODE	LD P			TO B		10	EXT			STRU	0 N T A	+100	SNI	- 1	-	SB	EAR	En B					HIS	3	200		UIIN	0 N O							
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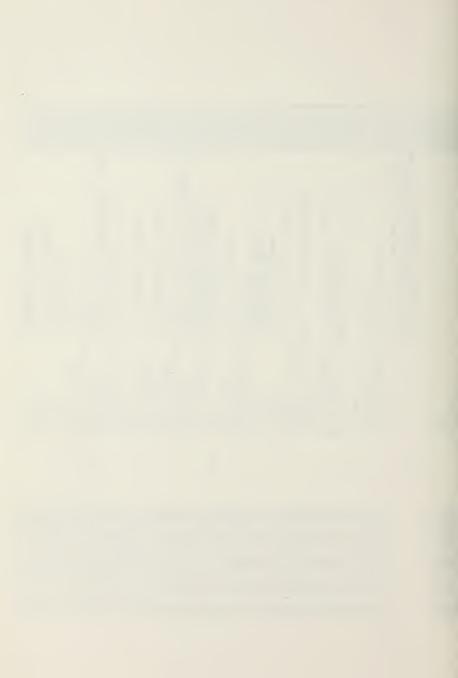
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N HII PUS. 26 IN INE PON	END CARRY ROUTINES * * * * * * * * * * * * * * * * * * *	CONDITION CODE SETTING	× 0	THE FOULTHE TESTS THE CENTENTS OF THE STATE OF AN A CHILL OF AN A STATE OF THE STATE OF STATE OF THE STATE OF
28 = SAR A1 OR 1 = A1, CSAR A1 C = A1 JUHP	CLEARBUIFI CLEARBUIFI AMPCR = A2 0 = 8C0.LCIR COMP 16 = SAR131 = L11 L11 = MAR2 PRINT UPF = L17 8 = MINUFF = L17 9 = MINUFF = L17 PBUFF - 1 = CPCR STEP JUHP	# # # # # # # # # # # # # # # # # # #	FALSE THEN A.D.	SFICCA: 1F LC1 THEN SKIP 10 L = 0 10 L = 0 10 L = 0 11 F LC2 THEN SKIP 11 F ALSE THEN BI SK 12 F ALSE THEN BI SK 12 F ALSE THEN SKIP 13 F ALSE THEN SKIP 14 F ALSE 15 F ALSE 16 F ALSE 17 F ALSE 18 F ALSE 18 F ALSE 18 F ALSE 19 F ALSE 10 T T T THEN SKIP 10 T T T THEN SKIP 10 T T T T T T T T T T T T T T T T T T T
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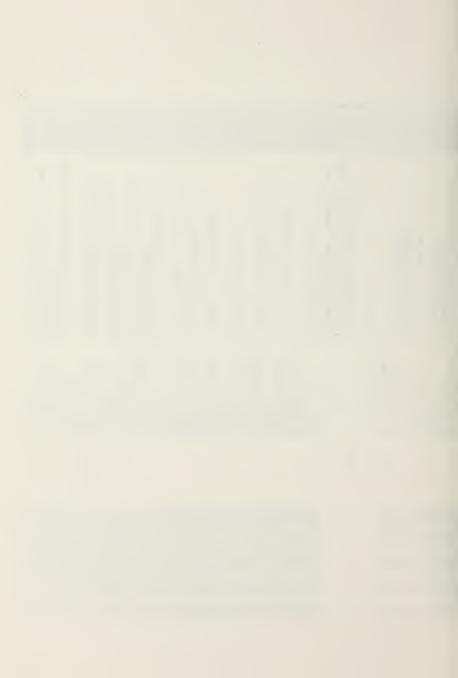
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	R ARITHMETIC TEST < 0 (NEG)		M JUST TO PLEAR FLAG SET IN SETCE					# IN SITE 20.25 OF THE PSV							S ROUTINE WILL SET CONDITION COPE		A ARITHMETIC TEST > 0 (POS)									~	1	A CODE BITS IN THE LS 2 BITS OF B	SHIFT CC BITS TO LS 2		ISOLATE	RESTORE A1			END CONDITION CODE ROUTINES* * * * * * * * * *			A ASSUMES THE INSTRUCTION IS IN B. THE		:	A INSTRUCTION IS PASSED IN B	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1305715 115		% PUT ADDRESS OF R(A) INTO B	MINVE ADDR OF REAL TO MS WORD		M UPPER WOFD OF A3 HAS ADDR OF R(A)	(RCA)) IS IN B	# RESTORE PETURN ACORESS				X THIS ROUTINE GETE (R(M)) IN E. IT	ASSUMES THE INSTRUCTION IS IN A			
	SETATE BIOLC = 8	8 # SAR	IF LC1	B OR A1 = A1	JUMP			SFT00:			0010 5 8		B AND A1 = A1	JUNE	SET01:			6100 R = 8	B ≈ SAR	B OR A1 = A1	B311 C = B	7 = SAR	B AND A1 = A1				CHECKCCs		A1 C = A1 C CSAR	16	¥	A1 C = A1	ЧÞ		THERM WHEN END CONDIT		CONTENTSRA:			MP CR					B = B		COMP 16 = SAR	B 0R A3 = A3	FINDIT - 1 = CPCR		PHUL			CONTENTSRMs		AMPCR = A2	A3 AND LIT = B	15 = LIT
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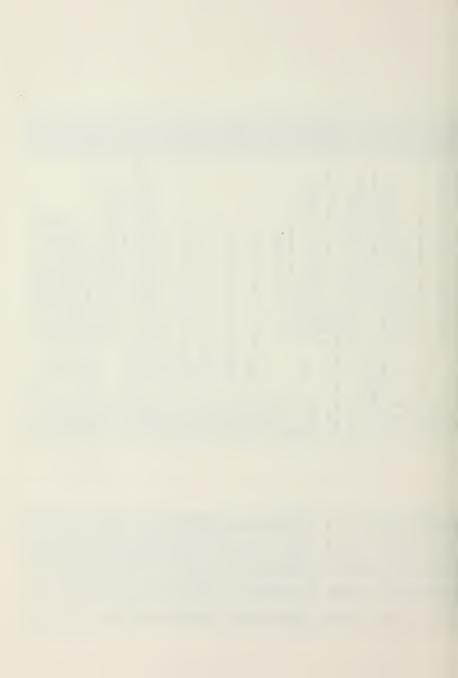
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REGSIACK - 1 = CPCR E NPUI - 1 = CPCR E NPUI - 1 = CPCR S TR S TR S TR I HIS ROUTINE VILL DIVIDE A276, AND I THE CUOTIENT IS RETURNED IN A3, EEM IN A A2, ALL UNHERS AUST BE LEFT JUSTIFFED A LC. MUST BE SET FOR REG PAIR OF YOURNE	S NE	F TRUE THEN STEP ELSE SKIP 8 CHECK FOR ZERO DIVISOR UVERFLOW	A 2	1
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S CHECK FOR A 16 BIT QUOTIENT		ST STEP ELSE JUMP 4 LC2 = NEG QUOT.	COMPLEMENT GUOTIENT	CLEAR UHW OF QUOTIENT	DIGHT HEFTEN ONSTRUM		CONTRACTOR AND		RIGHT JUSTIFF REPAINUFE	AZI SIEP ELSE JUMP		_	* DEBUGGER * * * * * * * * * * * * * * * * * *		I THIS ROUTINE WILL DUMP OUT THE	FRULATORIS MAIN REMORT MAPPING THROUGH	THE RIC ADDR AND THE FOLLOWING	I D-MACHINE REGISTERS: AHFOR, AL, AZ,	A3, FIR, AND BRI	SAVE MIR IN B REGISTER	I SAVE AMPCR			A WRITE AMPER INTO WORKSPACE			A STANTO CONTRACTOR	TO LEVEL TO THE TOTAL TOTAL		T URITE AD INTO UNDERCRACE . 2	TO THE SET OF THE STATE OF		T WRITE AS INTO MORKSPACE . I			M WRITE MIR INTO WORKSPACE + 4		X REFERENCE BR1			A WHILE BRI INIU WURKSPACE + 5	A MO HOLD S READ ADER	N USF FRI AS HOLDER OF REAL ADDRESS	A CLEAR PRINTBUFF	R SET UP PEAD ADDRESS	PRINTBUFF ADDR TO BE WRITTEN INTO		A READ THE CONTENTS OF A GENERAL RFG			Chief ve on Control Chief ve of the Parish of the	A FOLE INTO ASP INTENCHANCE OF 16 DITS	C THERE HID AND B	A A 2 CONTA		R SHIFT AS RIGHT TO POSITION NEXT 4 BITS
	IF FALSE THEN SET LC1	NOT A3 = A	1 = A3	AS E MAS	2	C4 = C4 103	- A2	9	THE REPORT OF THE	COUDS SE LC2 THEN NOT AZ = A	A2 + 1 = A21 JUHP		* * * * * * * * * * * * * * * * * * * *	-	DUMPREGI					EHI	ANPCR = MIR	LIT = MAR2	WORKSPACE = LIT	· EOUTPUT - 1 = CPCR		A1 = HIR	oldo = 1		A2 = MIR	1 = CPCR		A3 = HIR	1 = CPCR		B = HIR	PCR	R + 1 = MAR2		BHAR R = MIR	S SAN		IT COME A =	= 6R1	NFXTEIGHT: CLEARBUFF - 1 = CPCR	A3 = MAR2 %	L17 = A1 8	PRINTBUFF = L1T	NEXTREG: EINPUT - 1 = CPCR 8	4	BIAK L = BK1	COLC = AT COLC			LIT = A21 IF		A3 R = A3
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AZ GTR LIT S CHECK IF 9 DIGIT HEX VALUE TE A-1	TE YOUR AND A LITE A AND CATED FILE CAMED IN ANY 1 CAD COL	AZ * LII - AZ OIET CLOC ONIT A AUI / TOR	A2 + 0 C = 0 S PLACE 4 DIGIT VALUE INTO BC HEX WORD)	CLAN H CC	00	4 = 111		LIT EOL B X TEST COUNTER FOR 4 ITERATIONS IF TRUE THEN SET LC11 STEP ELSE SKIP X TRUF HEALS HALFWORD	FOUTPUT - 1 = CPCR & COMPLETED-WRITE IT INTO KEHORY	1F LC1 THEN SET LC1s A1 + 1 = A1 % INCREMENT PRINTPUFF A0DR	IF LC1 THEN SET LC11 0 = B S CLEAR P FOR NEXT HALFWORD	IF LC1 THEN STEP ELSE SKIP M 16 BITS OF THE GIVEN REGISTER	DEALUGIST - I S EPCK AMAVE PELN CUMVERTED TO UCL FURNAL 4 DESTADE DADILLE D CANCIDICA	NOT COV THEN STEP E	×	S GENERAL	A1 = HAR2	# LTCR	R R = A3		A3 + 1 = A3 R SET UP NEXT READ ADDRESS	AS EOL LIT		AS EUL LITT IT TRUE THEM SET LOITSTEP ELSE SKIP WATTEBUFF - 1 = CPCR	16 = [1]	AS EOL LITT IF TRUE THEN SET LC11STEP ELSE SKIP	- 1 = CPCR		AS EUL LITT IF TRUE THEN SLI LC17STEP ELSE SKIP	3 = L = C7C8	A3 EOL LITT IF TRUE THEN STEPT SET LC1 ELSE SKIP	: - 1 = CPCR	40 = 1.17	AS EOL LITT IF TRUE THEN STOPT SET LOT ELSE SKIP WRITEBUFF - 1 = CPOR	A3 = HAR2 & MAR2 CONTAINS ADFRESS OF NEXT REG.	N STEP ELSE		A1 + LIT = A1 K PUT SPACE BETWEEN REGISTER VALUES	A 1 FO 117 S CHECK 1F ALL REG MANE RESN'OUMPED		TRUE THEN STEP ELSE SKIP	1 = HPCR %	- 1 = CPCR %	CLEARBUFF - 1 = CPCR % CLEAR THE PRINT FUFFER		- 1 = CPCR % JUST TO CREATE A BLANK	- 1 = CPCR % JUST TO CREATE A BLANK	HAR? TEOAD THE ADDRESS OF A1	WORKSPACE = LIT
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CONTENTS	CONSTRUCT ADDRESS		CONSTRUCT ADDRESS					0 F				A PUT ADDRESS OF AMPCR IN MARZ	READ IN OLD AMPCR	AMP				THIS ROUTINE READS THE CONTENT	PERFORM READ	READ CONTENTS OF MAR? INTO			A THIS ROUTINE WRITES KIR INTO THE	MEMORY ADDRESS OF MARZ	0	A WHEN WRITE CORPLETER		THIS ROUTINE DOES EXTERNAL 1/0	INTERFACE BETWEEN THE UYK2" EMULATION	AND THE 10P. B CONTAINS THE CONTENTS	-			INTO MATEROX							THIS ROUTINE PRINTS OUT THE FRROR	HESSAGE "FAULT INTERRUPT"	INSERTED BY LOADER JCL AND				CHEALE ERRUKLISI AUUKESS IR			
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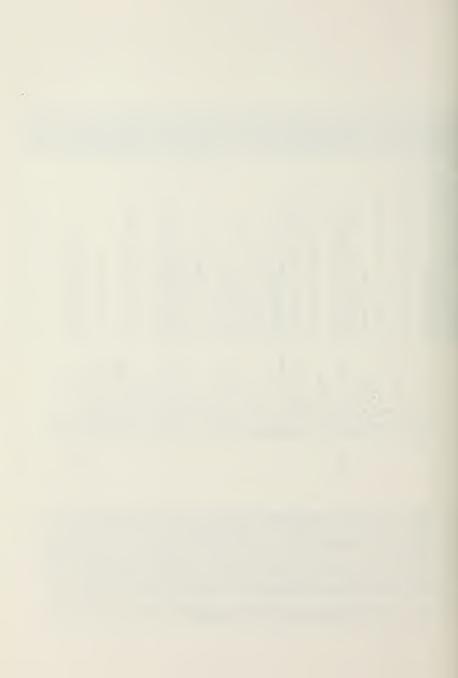
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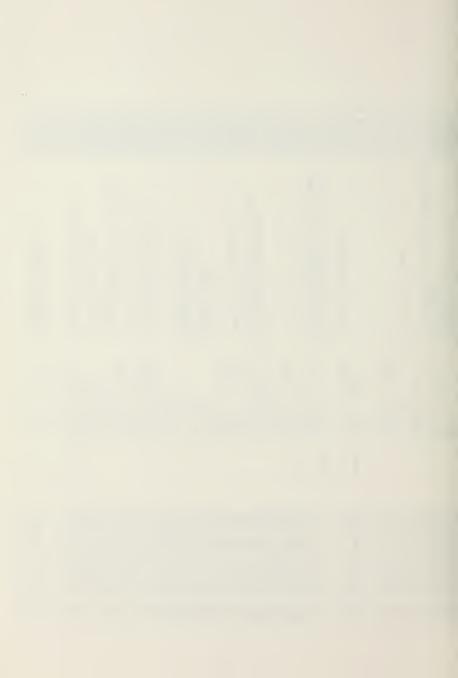
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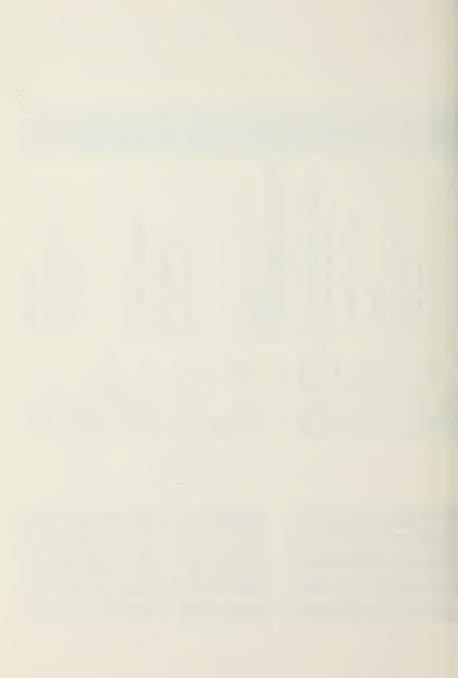
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MIS RUUTINE WILL TAKE A BUFFER	CONTAINING 32 BIT WORDS AND EXPAND EACHO1199COD	INTO 2 - 32 PIT WORDS, PUTTING THE INFO0120CC00	THE LHW OF EACH 32 OIT WORD.	BR1 MUST CONTAIN THE BUFFER ADDRESS	AND AS HUST CONTAIN B OF BUFFERS/COUNT			A ISOLATE THE COUNT(BUFF EXPAND FACTOR)			CALCULATE FIRST OUTPUT ANDRESS		RETURN IN BR1		+ -	CONTENTS OF 1 WORD INTO C	RU CUNIENIS INTO USIN UF AZ		ISOLATE BUFFER COUNT		BUFFER ADDR + COUNT INTO BR2	Control of the contro	REFERENCE MARY		ISOLATE THE COUNT		COUNT INTO B	NEXT READ ADDRESS INTO BE2	9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		REDUCE THE COUNT BY 1		NEXT WRITE AFORESS	WALTE OUT NEXT EXPANDED WORD	REDUCE THE COUNT			A CHECK IF ALL WORDS EXPANCED			NEXT READ ADDRESS			FERENCE MR1	RESTORE RETURN ADDRESS					THIS ROUTINE DUMPS THE EUFFERS
1	CON	Z	z	BRI	N N			150			CAL		RE		906	000	0		1 8 0		BUE		RFF		180		000	ž	1	Z L		RED	1	N N	N9	REC			СНЕ			E Z			REF	RES					Ξ
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					854	DINAR R = 42	N.	A3 L = B	COMP 16 = SAR	D R = B	A2 + B= A2	A2 - 1 = A2	AMPCR L = BR1	COMP 8 = SAR			1	AS R MIRE ASE		A2 R = A2	A2 + BHAR L = BR2	2000	4	BHAR = A2	A3 L = D	COMP 16 = SAR	0 = 0	A2 - B L = BR2	CURP 8 = SAR	B R = MIP	16 = SAR	A3 - 1 L = A2	A2 R = A2	A2 + BMAR L = BR2 COMP A = SAR	EMULOUT - 1 = CPCR	A3 - 1 = A3	A3 L = A2	A2 R = A2 B	AZ EGL 0	IF FALSE THEN SKIP	EXPEND - 1 = HPCR	A2 - B - 1 L = D82		EXPRPT - 1 = MPCR	ASR	BHAR R = AMPCR	OB II SAR	STEP	June		
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INDICATED BY THE BUFFER ASSRESS TO	PRINTER, CRI, OR DISK (NOT IMPLEMENTED)	MAR2 = 10CW	REFFERENCE OR2	100% + 1	B = (IOCN+1)			A2 HAS DEVICE CODE								DISK IO NOT IMPLEMENTED			COMPRES DIFFER TO 30 DIT 1 AT LE	BHEEFE ACRES TO MID						ER ADUR.	BUFFER LENGTH INTO B (HAILBOX-1)	TOANCEED DUCKED LENGTH 18 TO A 2	TANETER SUFFER LENGTH INTO AZ		SAVE AZ IN MIR	ISOLATE COUNTER			DECKENENT COUNTER IN AS			TEST THE COUNTER FOR ZERO		REGENERATE BUFFER ADDRESS IN B		LEMETE. 43	E - BOFFER LENGIFF AZ - FOFFER ADOR HULTIPLY B BY 2	*	NEW BUFFER ACOR IN BR1		NEW EUFFER AFORESS IN 10CW +1			WRITE PRI FUNCTION	COMPRESS THE BUFFER	REGENERATE BUFFER ADDRESS	
*	×	~	× 1	× :	# B	n K		*					w			×			× •		,					×	×				υ κ			× 1				×		et et					2		z K						
		1F LC2			EINFUL = 1 = CPCK	COMP & CAD	A 2 R H A 2		2	DUTDEV - 1 = AMPCR		EXEC		- 1 =	==	NOTINP - 1 = MPCK			SEI LC2	111 + 1 = HAR2	10CW = L1T	EINPUT - 1 = CPCR	P = HIR	LIT L = 681	7 = LIT; COMP 16 = SAR		BHAR + 1 = HAR2	-	10C10 - 1 = CPCR	1	IR	œ	S I	-	A3 C = A3	# ن	AZ EGL O	IF FALSE THEN SKIP	OPCODE - 1 = MPCR	111 + 1 = HAR2	CINDIN = LII	D = 43. DM1	B L = B 611		8	COMP 8 = SAR	2 + B = MIR	SPACE TO THE CPCR			COMPRES - 1 = CPCR	LIT + 1 = MAR2	10CW = LIT
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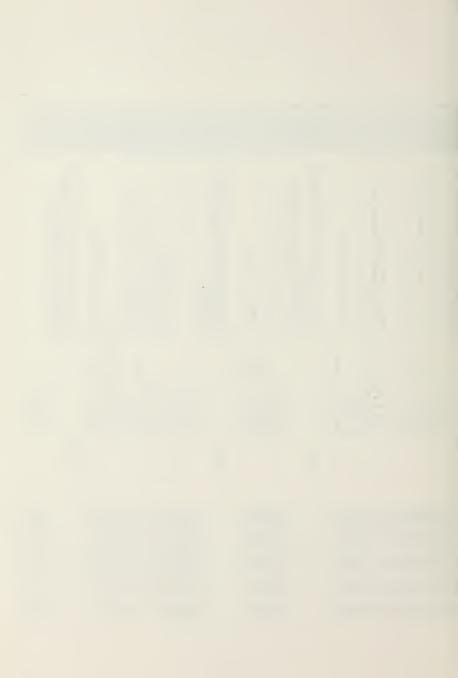
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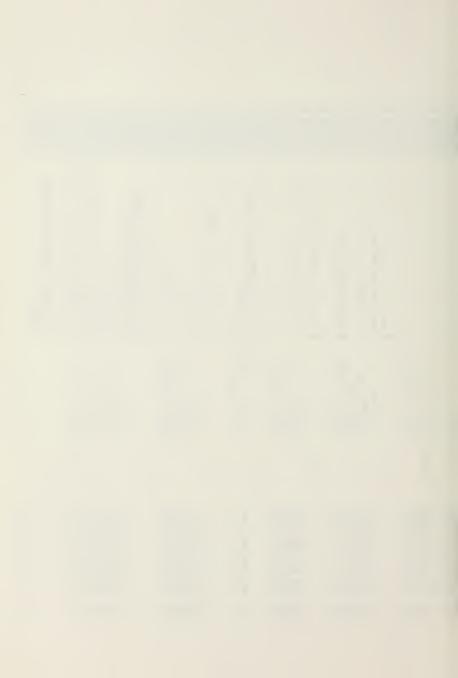
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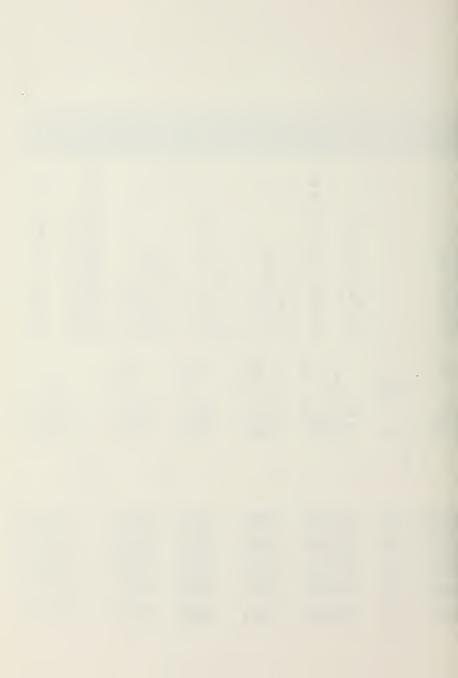
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A INI A! T = 1T3 + (R(H))	K LC2 INDICATES BYTE INSTRUCTION	K ROUTINES RETURN B = Y				0 1 1 1 0 0	31111		CLEAN UNW DF			Anti		A LHW OF AS CONTAINS INSTRUCTION	K B = (R(H))	A D CONTAINS .Y.			CALCULATE ADERESS OF								RETURNS P = Y										I THIS ROUTINE READS IN IN1 AND TESTS			The state of	CLEAN ONR OF				N BR2 = IN1 ADDRESS		SAVE							BIT	811					I LOCATION OF THE INDIRECT WORD	A A2 IS BIT MASK FOR J FIFLD OF IN				
			LIT = MAR2	STACK = LII	AS = MIR	OCOC - + INDING	2000 1 101001	-	A 3 L = A 3	COMP 16 = SAR	A3 R = A3	G = G			13	A & D = A2		I O H SAK						IAWOII					2 W 2 2 2 2 2 2 2 2 2	SIACR ELLI	AIR = CA	FOUTPUT - 1 = CPCR		INDIRWD - 1 = MPCR			INDIRWOS				2 1 2 2 4	COMP 16 = SAR	AS R B A3	B L = BR2	COMP 8 = SAR			A3 OR B = A3	FMULIN - 1 = CPCR	B R = A2	14 = SAR	A 2			DIRECT - 1 = MPCR			CASCADED:			8101 C = A2	19 = SAR	"		
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	01439000	NSTRUCTION 0144 CC00	X MA AT Y = TY1 + CR(H) 0149500 1	1 14 AT 7 = 171 - (REL) 01435000 1 LO2 INDICATES BOYE INSPUCIION 014407000 1 ROUTINES RETURN B = Y 014421000 014421000	MAY AIY = 171 + CR(H3)	1914 T = 171 = (R(Th))	1	THAIN	1	1	1	1911 1 1 1 1 1 1 1 1	1911 1 1 1 1 1 1 1 1	19 17 17 17 17 17 17 17	11	19 19 19 19 19 19 19 19	19 1 1 1 1 1 1 1 1 1	1	1	11 11 12 13 14 17 17 17 17 17 17 17	19 19 19 19 19 19 19 19	11 11 12 13 14 17 17 17 17 17 17 17	19 19 19 19 19 19 19 19	11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 11 11 11 11 1	11	11 11 11 11 11 11 11 1	1	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 11 11 11 11 1	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 12 13 14 17 17 17 17 17 17 17	11 11 11 12 13 14 17 17 17 17 17 17 17	11 11 12 14 13 14 14 14 14 14 14	11 11 12 14 15 15 15 15 15 15 15	11 11 12 14 13 14 14 14 14 14 14	11 11 12 13 13 14 17 17 17 17 17 17 17	11 11 12 13 14 17 17 17 17 17 17 17	11 1 1 1 1 1 1 1 1	11	11	200 OCTO CORGO CONTRACTOR AND	200 0000 0000 0000 0000 0000 0000 0000	200 OCTO DOEO	10 10 10 10 10 10 10 10	10 10 10 10 10 10 10 10	10 10 10 10 10 10 10 10	1	CLC2 NOTICE ONE CLC2 NOTICE SETURN STACK CLC4 NOTICE SETURN STACK CLC4 CL	COUNTY C	COUNTY CONTRICT CONTRINES CONTRINE	CALCADE CORP. CASCADE CALCAD CALCAD	COUNTY C	CALCACAGE CASCAGE CA	CALCADE CONTRICT CONTRICT	CONTRICT CONTRICT	Company Comp	CONTRICTOR CON



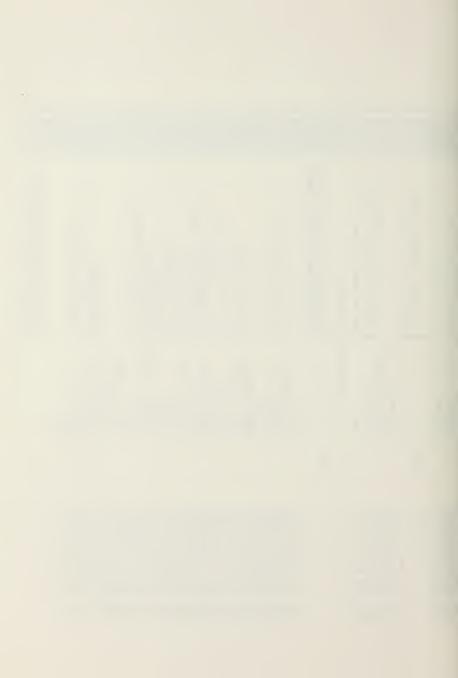
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01498600	01499601	01501600	01502000	01503000	01504000	01505600	01506	0100/0010	01208	01510	01511600	01512600	01513	2 2	01515	01516	01517000	01518	01519	01520	01521660	01523600	01524606	01525	01526000	01527000	01528	01529000	01530600	01531600	0155200	01533660	01554600	01536600	01517600	01538	01539660	01546600	01541600	C1542	01543630	01544606	01545000	01547600			(RCM+1))0155 CC 00	01551000	01552000	01553000	0155400	01555600	01556100	1
COMPUTE FORMULA PESTRED										NEW 1W AT Y = 1W2			EXT ADDRESS OF TV	The state of the s	CONTAINS IN21 Y = IW2	= PEXT ADDR OF INI		:	NEW IW AT Y = IW2 + (R(X))		CREATE RIGISTER ROAD	= (B(X))				& NEW INDIRECTWORD AT Y = IW2 + (R(M))	S A3 HAS INST. IN LOWER 16 BITS	R = (R(M))				NEW IN AT $Y = 1M2 + (R(H+1))$		4 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		= (8(H+1))				THIS ROUTINE COMPUTES Y GIVEN		SHIFT ADOR OF IW INTO A2	71 90 90 4 1 2 3	AUUK OF	SAVE (R(X)), (R(H)), OR (E(H+1)) IN A2		= (1W2) + ((R(X))), (R(M)), PR (R(M+	Y = REXT ADDR OF 141			THIS ROUTINE DECIDES WHAT ADDRESSING	ORMULA TO COMPUTE Y - FFF. UPERAND	AUDRESS	
2 %			×	×				,	٠.	2				•		* *	×		2		K	•	t	~	•	z	CP CR X	E *		er i		z			ŧ			×	set.		æ	SO BR								×			*	
HPC	1 - 1 =	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2			- 1	10 1	10)I			0 24	2		- Y	FAULTN - 1 = CPCR					8 AND LIT = 8		CINDUT - 4 = CPCR					CONTENTSRH - 1 = CP		ADYF - 1 = MPCR				A3 AND LIT = 8	15 = L11	,	- 11						AS R = A2	-	1 Y	B = A2	FHII IN - 1 = CPCR	1 65	,					,	6101 C = A2
					IMADDR 1					ADTO									ADT11							ADT2:						A013:								ADYF:											DIRECT:			
0 00 0	0000	0 0 E O			0040	0040	0040	040			0 10 0	0000	200	0 10 0	0900	0040				0.000	0.05.0	0900	0000				0900		0040				000	000	0 70 0	0900	0000					0 C E 0	0020	0 10 0	000	0 9 0 0	0000	0040						: A + O = 0
0640	0000	00.00			2000	00 00	0000	0000			0	0000		0000	0000	0000				0830	2000	05.00	0000				0000		0000				0836	2000		0000	0000					A00r	0000			0000	96.80	0000						4809 18C1 AC30 COFC
		0000					0000				00.5									2056							0000		0000				E156											0000										1901
4809	0796	4809	0		07 A O	0780	0700	0700			000	4809	2000	4000	07 F.C	4160				4809	0010	0770	0800				2380		0810				1809	GADO	000	2 F 1 C	0830					4809	0000	4004	2000	080	8800	4160					000	4004
042A	0428	0420	03 60		042E	042F	0430	0431				25 50	0000	0434	66.45	C437				C 4 3 8	0439	04.3A	0610	2			0430		· 043E				043F	0 0	4 1 1 2	2000	0444					5440	9 1 1 0	/ 5 10 10	0 4 4 0	0 0 0 0	0.449	0440					0	0440



01558600 0	0.0			01562600 0		000	01545404	2000	0.1366000	000/	01568000 0	0 1569000 0	0000		_	01573000 0	01574000 0		0000			_	_	_	_ 00 J	01582C00 D	01583000 0	01584C00 D	_							01592C00 D							_		2002			010020010	100/000	01606000 0				2002	3 0 0 0	000	00.5	01616000 0	0 0001100	
MASK : J: FIELD OF IVI		BIT VALUE IN A2	COMPUTE JUMP TABLE ADDRESS 0	HULA DESIRED													SHIFT ADDR OF 1V1 INTO A2					2	DITUIL SELV LLZ = NS BITE	0	0		= 1 W2 + (R(X)) 0	0	ISOLATE RX FPON IVI		= (R(X))				0 ((U))) + 2M1 =		MASK UFF INI FIELD INI = KM C		= (K(H))		0	= 1W2 + (K(H+1))		RA INTO B						-		200	INTO BRZ INL. FT 1	0	0		VE TREADURERING UNTREMETED IN AZ	= (IM2)	D	
# SAR	AZ AND B R = AZ	II SAR	* AMPCR = AMPCR *	DR - 1 = AMFCR X	STEP	EXEC			0.001		1		D13 - 1 = HPCR	-		*			A2 OR 1 L = BR2	P R = SAR	9 0000	e cres	2	UINCIUKN - 1 = MICK			* *	B AND LIT = B	15 = LIT 8 19	- 1 = CFCR	- 1	MPCR					5 - L11 x	A L SECTOR	H :	DIGN - 1 = MPCK	** (A = 11	15 = [1]	0000	1 1	*				i a		2 × 1 × 1 × 1 × 1	10 1 00 1	-		e 1	1 = CPCh	X = 1	
									.0004010	00410						1010											0.11:					_		0.121	• • • • •				•			 1013							OTONO											
0000 00					0 100 u	0 000 0			0000				00000				0 00F C	0 0050	0 COF 0									0 00FC		0900 1						0 100						0 100		0 0 0 0 0								0 20 3								
0		0000 0000	0400 0690		0000 0000	0000 0000			0000 0000			0000 0000	0000 0000				EOC3 ACSC	0000 6000	0100 (000									2055 0630	0000 0000	2000 0000		0000 0000			0000 7513	0000 0000						00000	3000 6513									2004 0000								
3000	4809	3000	4809	0850	4809	4824			0 7 8 0	0000	0 / 90	0880	0680				4809	0000	4809	0000	0880	2000	0000	0000				4809	00F0	0980	2F 30	0800			0000	4000	OBE	3010	00.42			0000	200	0 0 0 0	0000	25.30	0000					0000	0000	0000	6000	0 0	200	0000	401	
3446	044F	04 20	0451	0452	0453	0454			2000	1000	0426	0457	6458				65 10 3	045A	0458	0450	08.00	0470	1 1 1 1 1 1	10				0900	1940	0462	C463	h9 n 0			27113	2010	0467	9750	000	0407		4 7 11 0		0 0 0	0000	000	PARE					07.00	0474	0872	2/10	2 2 2 2	2 2 2 2 2	27.00	2	



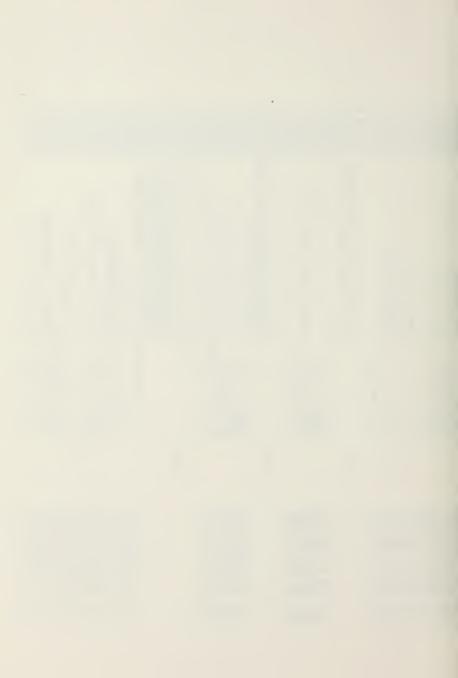
	C1619000 0		01621000 0	01622(00 0	01623C00 C	C1624C00 P								01632(00 0		01634000 0				0.0000000000000000000000000000000000000									01647100 0					01022100					01658600 0				01662000 D	01663(00 0	01664(CO D	01665000 0		_		01569(00 D	_	01671600 0		016/3000		01676606	01677C00 P
S. A.D. H. BERERRY, (DENNY, CHEMIST)	EP ELSE SKIP	GYTETEST - 1 = CPCR x DO BYTE FUNCTION IF LC2 EET	X 8 = X		~			RXMF IELD FRIERS WITH B =	X A2 = Y			A READ IN CONTENTS OF STACK	A RESTORE RETURN ADDRESS IN AMPCR	> = c	S JUMP TO EXMITELD CALLER	_	****	K I DAN DOHELFE	DOUTING TAKES AS THEM	A THIS RUDIINE TARES AS INTUL AN AUDIC.	K INTO DA DA 44			SA SO HAND IN HON SA SA	SATE RETORN IN ON OF	CANT Y OD Y IN AD			C (Y) OR (YE) INTO B	DRO DAS YE AT DR		2 - 2 - 2 - 2 - 2 - 2 - 2 - 2 - 2 - 2 -	AZ = (I ") ONN OR (I)	20 (0112) = 0		* AZ = (1*)/(1**1) OK (1)/(1*1)			S (Y) GB (Y*) INTO HIR		R R(A) INTO MAP2	K (Y) OR (YW) INTO 9(A)	M SET DOUBLEWORD ARITH COMFARE						R (Y*+1) INTO MIR		& RETURN ADDRESS IN AMFOR				S MOVES THE NUMBER OF CELLS SPECIFIED	BY UNW OF	R INTO ADDR LOCATED IN LHK OF A3
R E A2.BHI	IF LC2 THEN SET LC21ST	GYTETEST - 1 = CPCR	A2 + B = B	DIRETURN - 1 = MPCR			OTRETURN:			LII = MAR2	STACK = LIII 16 = SAR	EINPUT - 1 = CPCR	B R = AMPCR	A2 = 8	JUMP		S * * * * * * FND INDIRECT WORD ROLLINGS	IDBLE				7 7 7 7	COMP 16 = SAR	TO THE CO	2	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2		2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	CPCR		346	2000		0707			SAR 15 = 11T		,		STACK - 1 = CFCR	T - 1 = CPCR		SET LC1	SETCCA - 1 = CPCR	A2 L = A2	117	R = MAR2	A2 R = M1R	= CPCR	= AMPCR	STEP			MOVE:		
4809 0540 2030	3846 0000 0090	1E1C 00C0	4809 CC40 CB1C	0936 0000 6000 0040					4809 0040 2000	4809 2003 0010	0000 0000	2F3C C0C0 0000	4809 0040 8040	4609 CCAO 0830 00FO	4820 0000 0C10 00F0								0000 0000 0000	UBOG EKEC 1000	4809 5001 9036	UB 09 0 C 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	OC 41 CC 10	2000 0000	0.30 0.00 0.00	4809 COD 0010	100 0000 0000	8899 0781 3000	2002 1200 0000		0000 2322 0000	4809 FORD 8030	90FC 0C03 0C00	4869 2655 6860	4809 Crin Brish	0000 0000 0000	0000 0000	0000 0000	4809 CDC0	4609 6000 6000	2000 0000 0000	4809 COC1 201C	0010 0000 0000	4809 2F5C 0C1C	4869 6000 8080	2550 0000 0000 006	4809 EOCO 8C40 OOF	4809 0503 0030 0050	100 0500 0000 0000				
0877	0478	6419	C47A	6478				-	0476	0470	0476	047F	0480	0481	0482							0.083	OGBE	0.00	0486	0.487	CUAR	0 0 0	0484	DAAR	0880	04.80	0000	0.195	0000	C491	0492	0493	649	6495	96 00	6497	0498	0499	049A	0498	0490	06 60	049E	C49F	C 4 A D	0441	- 1				



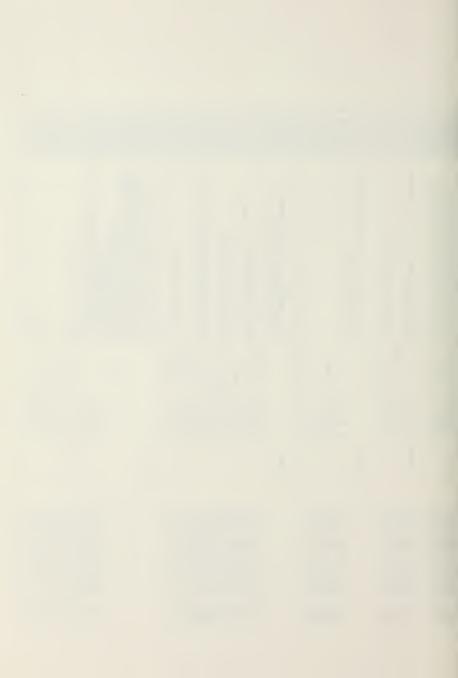
0 0000000	01679000 0	01686600 0	01681000 n	01682000 0	3005	000	200					_	0 00 00 00 0	01691000 0	01692000 0	01693000 C		0000				_	_	_	_	01762600 0	01703000 0	01704000	01705000 0	01706000 0	_	_	01759500 0		01711F00 D	01712C00 E			C1715C00 B	_	C1717C0C D	D01718COF D			1000						_						01733C00 f	_	01735000 0	01736600 0	01737000 0
PAGE ADDRESSING IS ALLUMIU	SAVE RETURN IN AZ			i 6 = (8R1)	TRANSFER B TO MIR		22		K ZERO DUT I HW OF AN		0		STURE ARPER IN LHW OF AS		S STORE AMPCR IN UHW OF A2		RETUPN AMPCR TO LHW OF A2	7500 1410 05 44				STORE DESTINATION ADDR IN LAW UF AS	5		INCREMENT ORIGIN	SHIFT COUNT TO LIN OF A3		DECREMENT COUNTER	ISOLATE COUNTER IN LHW OF B	0	RESTORE A3			ELSE SKIP	c	0	C	0	E.			THE OPERANDS MUST BE PASSED BY AZ AND	LC1 HUST BE SET 1F 32 BIT NUMBERS ARE	PASSED. PRODUCT IS RETURNED IN A3.	# HOLDS PARTIAL PRODUCT 0			& DOUBLE PACK SINGLE REG VALUES 0		K FOR NEG PROD	KUDUCI		TWO:S COMPLEMENT	ERING 9 TO THE ADDER	S COMPLEMENT 6		RESTORE SINGLE REG TO LS WORDS	BRING A 2 TO THE ADDER		SHIFT OFF LS BIT OF A2	3
*	AMPCR = A2		0 8 2	EMULIN - 1 = CPCK N	R a MIR	A2 = B	A 5 1 = BR2	COHP & CAD		CAP	200	A3 E # A3	AS UR B B AS	OUT - 1 = CPCR		COMP 16 = SAR		2 4 4 6 5 4) M	0			DILAR N = BICCAN		B + 1 L = PR1	m	16 = SAR	A3 - 1 = A3,8 S	L = B	E R = 8	A3 C = A3 K	8 E 0 F 0	COMP 8 = SAR	LSE THEN STEP	MRPT - 1 = MPCR		STEP	JUHP	*	*	*						LCII	I = MPCR	r EOL 8	IF FALSE THEN A2 XOR B1	AZI IF USI IHEN SEI LCZ	F HSI IHEN NOI AZ = A	2 + 1 = A2	•	IF HST THEN 0 - 0 = B		RREG - 1 = MPCR #		¥ = 8 +	A2 R = A2 CSAR K	1 = SAR
		HRP I s																																							HULTS								CHOLS								,	MULT1:			
		0000 20F0			0C30 00F0		CC10 COFO									0000 0000	A C 0 0 0 0 F 0													8800 00F0	9000 00F0	0030 00F0	0000 0030		0000 0000	Or4r 00F0		00% 00F0												0000 0000					0830 0050					A09C 40FC	110 6000
	0 593	0000	0 F 4 3	0000	0 6 7 0	0000	E 0 0 1	0 0 0 0	E000	0000		1000	E C 3 C	0000	EDC1	0000	0000	FOLO		0 2 11 2		200	0 0	0000	0.047	E 0 0 1	0000	E 30 E	1 4 2 0	0 0 4 3	Enr 1	0.052	0000	0 0 0 0	0000	0000	0000	0000							0000	0000	0000	0000	2 5 2 0	5 6 5 5	0.00	2 2 2 2	1000	0 0 0 0	2520	6 3 4 3	0000	0000	E C 4 0	0 0 0 0	0000
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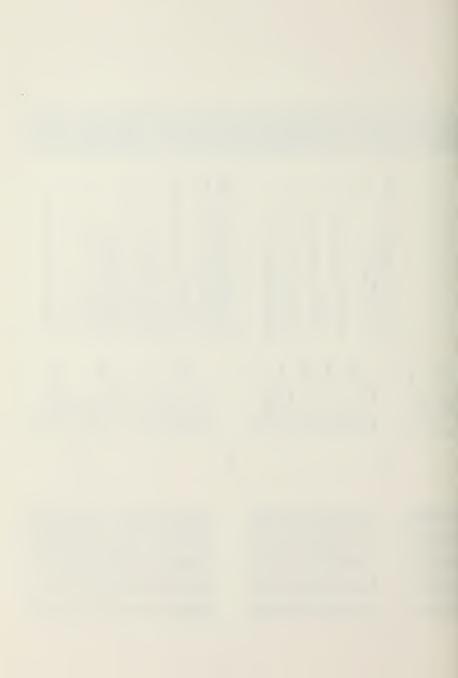
		0176700 0176900 017700 017700 017700 017700 017700 017700 017700 017700 017700	01782C00 01782C00 01782C00 01784C00 01774C00 01774C00 01775C00 017
* HULT HULTIPLIER EY 2 * CHECK TO SEE IF ENTINE HULTIPLIER * HAS PEEN REAC * IF HULTIPLICAND = 0, THEN DONE * AJSSTEP ELSE JUMP * HOVE 8 TO UMW 16 = SAR * TOON IN UNE HULT OP * RESTORE REG TO LHW *	THIS ROUTINE SETS UP AN ERROR HESSAGE "OLI IMPLEMENTEO" INSERTEO VIA LOADER JCL R CREATE ERRORLIST ADDR. IF DRI KINS ROUTINE WILL PRINT OUT AN ERPOR		SKIP R TEST FOR A SUBTRACTION OP COOF A A 2 TO THE AOCER A CHECK FOR "LINE" SIGNS SKIP R CLEAR THY OV BIT, UNLINE SIGNS SKIP R CHECK FOR NEG SUH NEG SUM, LINE SIGNS SKIP R OS SUM, LINE SIGNS, NEG X SKIP R POS SUM, LINE SIGNS, NEG X SKIP
A C E E E A C E E A C E E A C E E A C E E A C E E A C E E A C E A C E E A C E E A C E E A C E E A C E E A C E E A C E E A C E E A C E E A C E E A C E E A C E E A C E E B E E A C E E B E E B E E B E E B E E B E E B E E B E	NOTIMP: SAVEREG - 1 = CPCR ANTOR = 6 FRROKLIST = ANPCR FRROKLIST = 0 = 0 = 0 = 0 = 0 = 0 = 0 = 0 = 0 =	SAVEREG - 1 = CPCR RROOKLS B AROCK LIT + B L = RRI 16 = LIT COMP B = SAR P Q TERR - 1 = MPCR X = E E E E E E E E E E E E E E E E E E	F LC2 THEN STEP ELSE
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04009 04009 04000 04	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	C4EC 090F C 04ED 4809 C 04EF 6	CGF 2 200 B CGF 2



J 00																																																																	
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SUM LIKE SIGNS, POS		=======================================	=======================================	OTHERWISE, CLEAR THE OVERFLOW RIT			CLEA			KOV					LHE										*		LED	COOM POINTOUT IC CCMEDATED	CANON THE CONODINER WHEN	2			PRINTBUFF ADDRESS INTO		F A	INVE		01	MOTE COMPANIES AND THE THEORY	000			S				THIS ROUTINE CHECKS THE STACK	DESIGNATION EIT IN SR#1 TO DETERMINE	WHICH STACK THE PROGRAMMER IS USING	THE E REGISTER IS ASSUMED TO MAYE THE	DELATIVE DECISETED MINDED	7000			POSITION STACK DESIGNATOR BILLINGS	FUSILIUM REG BILLO IN LS FIL	œ							TAMBLE AS TO MODINAL CONSTRUCTION	
SIGN		INE	200	AR T			-			CHE					FIS	D C U											CAL	31		2		INE	Y DI		HA	BF.	,	SOUS	200	-			STEF				4ECKS	N	PRC	1.5			TED		01.5	:	ADDE							Made	
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N NEG	_	SKIP & THIS ROUTINE WILL SET THE	0 V E	-		_	Ξ	X 61T IN SRU1		A CLEAR I C1 FROM CHECKOV			×	_	A THIS ROUTINE SFTS THE OVERFLOW BIT IN	W POSITION 27 CC PSW									A 6	**	% THIS ROUTINE IS CALLED WHENEVER	100				A PRITE A BLANK LINE	S WR		10/1	A A VORDS VIII BE HOVED	t						# RES			_	H	N DES				107			200	Š	SE	SKIP				SK 16	5	9	Ú
						_	•		A R				_	_	_	•								1	j	_	_									SAR		•			2				•	•	•	•	_	_	•											IF TRUE THEN STEP FISE SKIP		•	•
нРСЯ		P E	MPCF	= HPCR					11,00	C 1										3 A F				-	E N D						. CP	= CPCR		CR		111			0			CPC "	CF	- 1 = MFCR														. E	CR			1 6 5			
1 1		2 2 1	11	11					B	15										1100					*						-	-		AME		HP		CPC			 	-	, =	11														STE	Ē II			2	,	-	
- 11		IF LC1 THEN STEP ELSE	SETOVBIT - 1 = MPCR	CLEAROV - 1			7	A.R.	8110	A 1 s	IIIMP								¥	A1 OR 1 = A1, CSAR	۷1				*						75.	WAITEBUFF - 1	AMPCR = A3	PRINTBUFF = AMPCR	8	A = IIII COMP 16	AT OR B = AT	and	1	STATE BOTH - 1 - COCO	4 !	WRITEBUFF - 1 = CPCR											00	, :	7	2		IF LST THEN STEP ELSE	STACK2 - 1 = MPCR	0	-			At C - At a LIMB	i
ETOVBIT		LC1	0 4 8	ARO			A1 C = A1	S	ONY	11	٥							1 4 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6 6	in	~ 0	۳ ن	JUHP			*						CLEARBUFF	I TE BI	CR :	INTBI	111 1 = 8	=	90		1 1 0		AKB	1 16 81	SREG	STOPTIME									N N		A1 C = A1	i i		LST	VCK 2	117 EOL D	11 = 111	TRIL	1000		د
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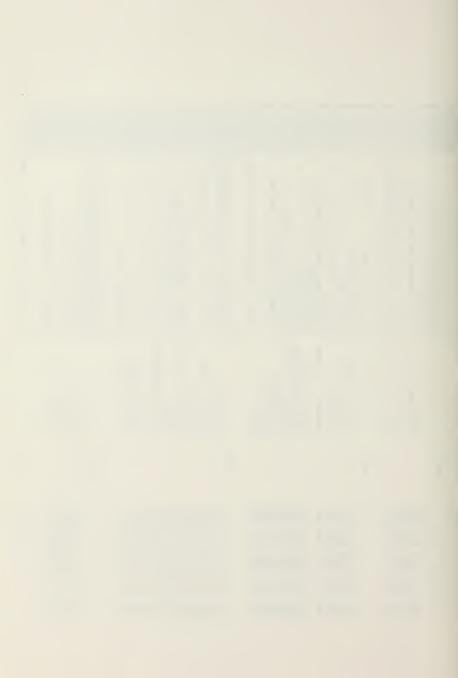
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	THIS ROUTING RESTORES THE REGISTERS OF THE LUI IN WORNSPACE SAVE RETURN IN HIR HAR2 = HORKSPACE + 1 HAR2 = HORKSPACE + 1 INCREHEN! WORKSPACE AOOR RESTORE AS INCREHEN! WORKSPACE AOOR RESTORE AS SELECT WORKSPACE BASE AOOR SWAP B ARO MIR RESTORE AS	THIS ROUTINE WILL PLACE THE CONTENTS OF FSW INTO THE PAR. THEN RESTORE SAVE RETURN AGON TO OPCOCE IN HIR AGORESS OF PSW (PSW) INTO B FIUNN AGON INTO B FAMILY HAS BELLING AGON INTO B FAMILY RETURN AGON INTO B FAMILY AGON INTO A PARENTAL PARENTAL BELLING AGON INTO A PARENTAL PARENTAL BELLING AGON INTO B FAMILY AGON INTO B FAMILY AGON INTO A PARENTAL BELLING AGON INTO B FAMILY AGON INTO A PARENTAL BELLING AGON INTO B FAMILY AGONT AND A PARENTAL BASEL BELLING AGONT AND A PARENTAL BASEL	RIGHT JUSTIFY (PAR) (PAR) + 2 = A2 (PAR) + 2 / PETURN AUDR = A3 CLEAR PAR (SSW) INTO PAR (SSW) INTO PAR CLEAR BIASEO FETCH BIT INSTAUTION AT Y INTO B CLEAR PAR (PAR) + 2 = F RESTORE RETUEN AOOR, INSTR IN B
w 1	NE SPECIFICAÇÃO DE SPECIFICAÇÃO		
STACK 21 (1) + 0 = DARZ 16 * (1) * (1) * (2) * (1) * (2) * (3) * (3) * (4) *	RESREG: AMPCR = HIR LIT + 1 = HAR2 WORKSPACE = LIT EINPUT - 1 = CPCR B = A1 = HAR2 EINPUT - 1 = CPCR B = A3 = A3 EINPUT - 1 = CPCR	ت ت	COMP 16 = SAR1 2 = L A2 R = A2 A2 P LIT L = A2 A2 P R = A3 A3 R = A1 A1 L = A1 A1 A1 L = A1 A1 A1 L = A1 A1 A1 R = B A1 R R R = B A1 R R R R R R R R R R R R R R R R R R R
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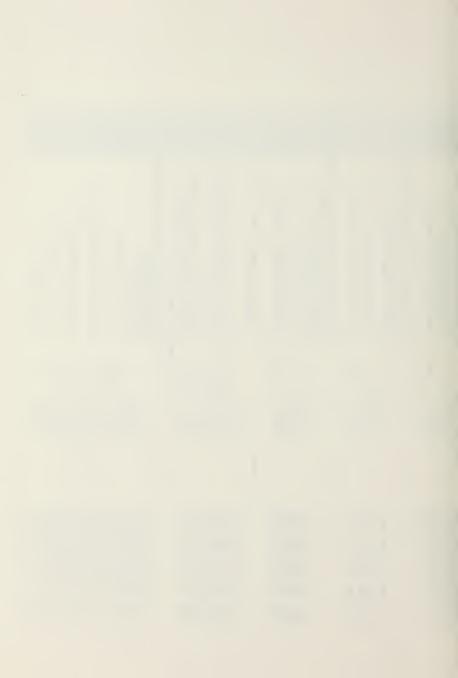
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% THIS ROUTINE COMPUTES (P)+ D = P % AND JUMPS TO NEXT INSTRUCTION	EXAMINE SIGN BIT OF "O"		A3 TO THE ADDER	R IF SIGN=1, FILL UPPER EYTE WITH 115	DESTORE "O" FIELD ID IS EVIE	2 - C-C-C-C-C-C-C-C-C-C-C-C-C-C-C-C-C-C-			SAVE THE OLD PAR IN MS WIRO OF A3	ALCCDRATION AND CPA & D		CLEAR ULU FAR		CREATE NEW PAR				THIS KOULINE GETS THE CONTENTS OF				SAVE RETURN ADORESS		SELFCT REGISTER		GET CONTENTS OF RCM)			000								A LITE AN INCIRCULORS CTON EXTRANCE		THE COCOLLAND INSTRUCTIONS				PREPARE ES 2 BITES UP AS TO HULD RETURNO17621JU		oregon as orthon appointed to the	MESTONE AS ACTION ACCUSATIONS	MASK UFF "M" FIFLU		K IS H = 0.1	SKIP	R JUMP TO DIRECT ADDRESS W/O INDEXING	K TEST FOR H = 1XXX			JUMP TO DIRECT ADDR WITH INDEXING	S CAVE B IN A2	SE SKIP	10 to	4 IF H = 10,12,14,16 THEN INDIRECTION
a I	A3 L = A3, CSAR X	24 = SAR	**************************************	HST THEN BILL I = 8	14 - 0	6			A1 L = A3			×	A1 L = A1	A1 OR B = A1 8	OPCODE - 1 = MPCR			KHI			A SE	AMPCR = A2 8	BMAR = B	ACK - 1 = CPCR		FINPUT - 1 = CPCG								S S S S S S S S S S S S S S S S S S S	* 1	RXMFIELU:	•	e 1	e s	e w			A5 C = A5	E 4 1 00014 00	1		AS AND LII = B N	_		P ELSE	= MPCR	-1	8 = LIT	IF FALSE THEN STEP ELSC SKIP	DAWI - 1 = MPCR K	B = A2	15 NOT LST THEN STEP ELSE SKIP		TADTR - 4 INDER
6	1030 0050	26.00	0000	r B 3 C	0000	0000	3340	2000	1030 COF 0	0000	2000	0000	400 COFC		0000						0000	2000	0800	0000		0900 0000			0000	2000	000												0.000 0.000		0000	26.26	0836	00100	00.00	0000	0000	0000	0000	0 00 00 00 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0 0000 0000 0	3 2030 COF 0			0000 0000
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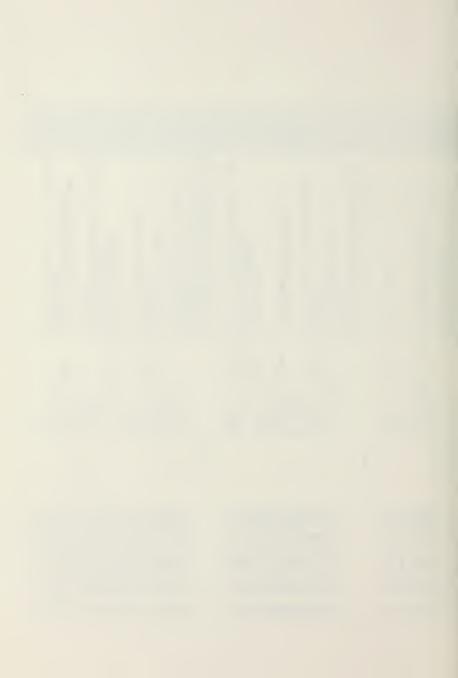
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A UTHCHMISER II - 11913913917 FLKFURN	* DIRECT ACDRESSING WITH INDEXING (RCH))		A THIS BOUTING BETTIBUS Y 18. D	241 110	S OF RXHFIFED	K B HAS Y	A RESTORE RETUFN ADDR FROM RXMFIELD		S CLEAR BYTE BIT, LC2=0; HSBYTE OF Y		× 1		# THIS ROUTINE FORMS Y = Y + (R(M))	N KILORNS I IN B	S GET NEXT ADDRESS		* MEINIEVE MELALIVE MIG. NO.	COURT TO SEE MARKET TO SEE THE	A COMPUTED ACTUAL LOCATION ON MAD		SIEP FISE SKIP	S CHECK FOR BYTE INSTRUCTION	K B HAS Y	S RESTORE RETURN ADDR FROM RXMFIFLD			S RETURN TO CALLING ROUTINE OF RXHFIELD		W THIS DONIENT SE CALLED IN MALE SECTION OF THE SEC	040		S READ SRAD INTO B TO USE CAM BOUTINES			LITS SKIP % TEST IF M = 10	O SR#2 "H" FIE		LITE SKIP & TEST IF M = 12			X TEST 1F M = 14		# DEFAULTS TO M = 16	guit 1				INDIRECT ADDRESSING	% ISOLATE :H: FIELD = 10		S B CONTAINS STATUS REG 2	SHALLOO SINJINGS ISSI OF OMIL &	A JULY TO TEST CONTENTS NUCLENE		A THIS ROUTINE WILL REHOVE THE :M: FIELD
U						IFEICH - 1 = CPCR	AS R = AMPCR	16 = SAR	IF LC2	2000					IFETCH - 1 = CPCR			13 = C11	-	FINPHT = 1 = CPCR	1 6 3	T - 1 = CPCR	A2 + B = B	A3 R = AMPCR	16 = SAR	STEP	JUMP			LET = MAR2	STATUS2 = L11	FINPUT - 1 = CPCR		8 = LIT	EOL		10 = LIT	FOL	SAM12 - 1 = MPCR	12 = LIT	IF FALSE THEN SKIP	- 1	SRM16 - 1 = MPCR						6101 C = A2		AZ AND B R = 9	COMITOR A POSS	1		
			DAVAL										DANI																TAIONE																	SRM10:									SRM12:
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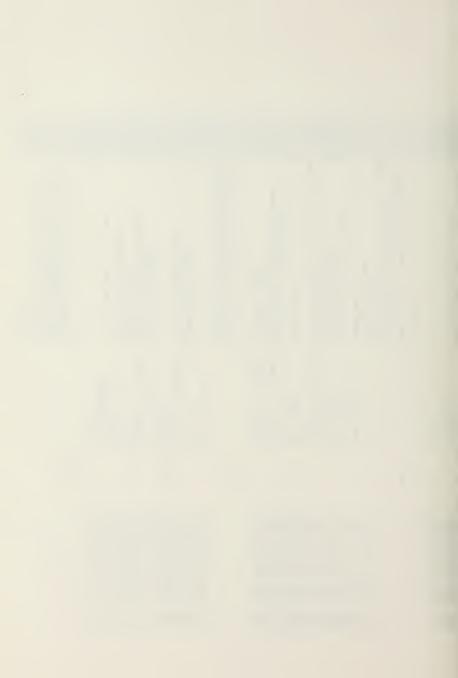
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FROM SRUZ AND CALL THE APPROPRIATE ISOLATE THE 12		B CONTAINS STATUS REG 2	P CONTAINS CONTENTS OF 181 FIFLD	JUMP TO TEST CONTENTS ROUTINE		į	THIS MUDITUR WILL REHOVE THE SHI FIELD	FAUR SHIPS AND CALL THE AFPROPRIATE	INDIPECT ADDRESSING ROUTINF	ISOLATE :M: FIELP = 14		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	U CUNIAINS SIAIUS WEG 2	A CONTAINS CONTENTS OF 1P1 FIFED	JUMP TO TEST CONTENTS ROUTINE			CLITT ON THE THE CHANGE THE SHETHOUS THE	THE MODIFIER WILL MENUAL THE SHIP FILED	FAUN SMIZ AND CALL THE AFPROPRIATE	INDIRECT ADDRESSING FOUTING	ISOLATE :M: FIELD = 16		B CONTAINS STATUS REG 2	B CONTAINS CONTENTS OF 11 FIFT D	JUMP TO TEST CONTENTS ROLLING				THIS ROUTING ANALYSES THE THE PIELD	CONTENTS M = 0.11,20,3			BISKIP & TEST CONTENTS OF "M" (0 OR 1)	ADDRESSING WITH		TEST IF "M" = 2	JUMP TO INDIRECT ADDR WITH INDEXING	INDIRECT ADDR VITUOUT INCEXING		FORMAT ROUTINES S S S S S S S S S S S S S S S S S S		THIS BOUTING SAVES THE DEST HATTY DEC.	DEFECTIVE OF THE CASE CONTROL OF THE CASE	C. C	בומנו פו וא שוויב			WRITE B INTO WORKSPACE			WRITE A1 INTO WORKSPACF +1			URITE AS INTO WORKSPACE + 2				WRITE AS INIC WORRSPACE + 3		RESTORE ADORESS	
0101 C = A2 K		A2 AND D R = B X		SANTESI - 1 = MPCR X	K 1			•	~	0101 C = A2 K	19 × SAR	0	D == == == == == == == == == == == == ==		SAMTEST - 1 = MPCR X	~		CRM16.		•		0101 C = A2 K		A2 AND B R = B K		- 1 = MPCR				SKILES I S		LIT GEO 9		IF FALSE THEN LIT EOL BJ	DAWI - 1 = MPCR %	2 = 111	JF TRUE THEN SKIP X	IAWI - 1 = MPCR K	~		A W W W W W W FND RX FORMAT		SAVEREGI	10 M	9	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2			MURKSPACE = LIT		EMAR + 1 = MAR2	A1 = HIR	EDUTPUT - 1 = CPCR	BHAR + 1 = MAR2	A2 = MIR 8	- 1 = CPCB		7 11 11	A S C HINE A S C C C C C C C C C C C C C C C C C C	ו ניונא	B = AMPCR	2
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			THE DOUTING STADTS THE EVICONAL		CLUCK UP THE 10P.		# PUT FUNCTION 2 INTO B	PHT START CLOCK FUNCTION INTO MID		000 1100	, ALL 101		STARL EXECUTION				CLOCK OF THE TOP AND INSTRIS THE TIME		INTO CLUCKLINE IN STRENON AND CALLS			4 PUT FUNCTION 2 IN B	CALL 10P	REREAD TIME	PUT CONTENTS OF MATIBOX INTO MIR		CLOCKTINE ADEDESC IN MAD.					READ IN SR #2	T SR II 2 TO THE ADDER	SKIP X TRACE IF TRUE	DUMP AN/UYK20 REGISTERS, ETC	RETURN TO LOADER FOR ADDITIONAL INPUT			THIS ROUTINE WILL PRINTOUT THE CONTENTS02133C00	OF PRINTPUFF TO THE CRT OR PTR	A2, MIR, AND B ARE USED IN THIS ROUTINEP 135000	SAVE AMPCR			ADDD OF COMP INTO MAD?				EXAMINE 2ND IS BIT OF SKE?				EBIT SKIP & CRI FUNCTION	R PRINTER FUNCTION	MIR CONTAINS 1/PRINTBUFF OR 7/PRINTBUFF02148C00	33 INTO 6		WRITE TO CRIZPIR 33 WORDS IN PRUFF							
JUHP			CTARTINE			111 L * B	2 = LITI COMP 16 = SAR	R H I OR R = MIR	11 = 1	dudu = 1	1000	000000	1	*	*	STOPTIME:					LIT L = MIR	2 = LIT; COMP 16 = SAR	EXTIO -* 1 = CPCR S	STOPTIME - 1 = MPCR X	B = MIR	LIT = MAR2	FILE STEELS	COLLEGE A COCO		2441 = 117		INPUT - 1 = CPCR		STEP ELSE	OUMPREG - 1 = CPCR X	NEWCARD - 1 = MPCR R		*	WRITEBUFF: R	~	*		BOOUT: LIT = MIR S	PRINTBUFF = LIT	A I I HARD	I Tr COMP 1			K		UHP 16 = SAK! 7 = LII		SI THEN [11 L = EB	= 681	B = MIR	LIT = B x	33 = L1T	CPCR	BDOUT - 1 = MPCR X	A2 = AMPCR	STEP				•
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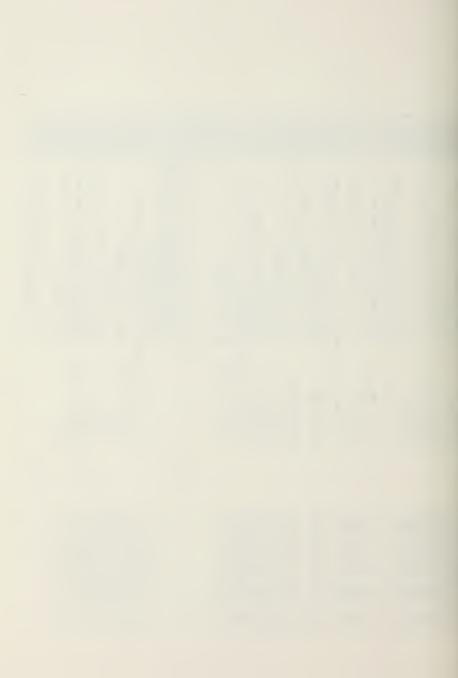
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A THIS ROUTINE WILL EXAMINE THE "F" CODE	FAN	"F" CODE IN LS 2 9175 OF A2				ROUI		BRF! STATUS LIT HAS BEEN SE! IN SKUI	BKI CONTAINS THE AUDKESS TO BE MATCHED. UZIOBCOU	A1.A2.A3.AMPCR MUST BE SAVED TO SE USEDO212000	SAVE AS IN HIR	REFERENCE BRZZHAR	SAVE BR2 IN A2		BREAKPOINT LOCATION IN MAR?	PERFORM PEAD OF EKPT	F CONTAINS BREAKFOINT	72		RESTORE PR2	-	FSTO	15 13	RETURN TO EMULDUI	RETURN TO EMULIN			THIS ROUTINE READS FROM MEMORY AFTER	CHECKING THE PAGING AND FREAKPOINT BITS02190C00	N S	RE READ FROM.			X SEND B TO THE ADDER	SAIP A LEST PAGING BILL	-		% SEND 8 TO THE ADDER	SKIP & TEST BREAKFOINT BIT	A JUHP TO EKPT ANALYSIS ROUTINE	EFF	SET UP MAR2 WITH ADDRESS	READ IN PRESENT ADDRESS					THIS ROUTINE WRITES OUT INTO MEMORY ACTER CHECKING THE PAGING STICRET 22)	AND THE PREAKPOINT BITS(EITS 21-70)	THE SRUI PORTION OF THE FSW. BRZ	NO	URITIEN.
×	2	er er			wt	FETCH ROUTINES	ue 1		K P						×	×	<u>~</u>	- u	9	2		*	STEP FISE SKIP & CALLING ROUTINE CHECK	×			. pc	ac.			er.	,	, ,			·		S			×	S)	*			ec :	y e !	- 4 - 4	- «c		× 1	- 3
						* FE								111				A FRZ FOUAL PRET							~										DE LST THEN STEP ELSE				IF LST THEN STEP ELSE													
			¥ 2			*								10			WHEN ROC THEN BEX	0 1 0	0				R = A21 IE IC1 THEN	MPC	= MPCR							LC1			ND P	** 0 - 0			1E P	BKTCHP - 1 = MPCR			RDC									
			91										A 2	BKPT	~	00	THEN	8 50	2	6	SAR		1		-	,					:	= 8; IF LC1		:	۰ د د	-			ENS	1		HAR2	4	THEN								
	= A2	AR	ח רו	=							014		11	ARI	HAR	IF R	RDC	ָר פּ'ר	-	a AR	1 00		21									18 =	SAR		Ξ .	ו ופ	0 4 0		H	- 4		" ~	AR RF x 1	RUC								
	A 3 R = A2	8 = SAR	AZ AND LII	117 = 6		*					A 2 HID	1 1 1 N	BHAR R = A2	8 = SARJ BKPT	LIT = HAR2	HR2# IF RDC	HEN	2 E0	TAL	- 6	COMP 8 = SAR	BHI	- 11	BKPTOUT	PKPTIN							~	= 22		2 2 2 4	2 0	≠ E	9	FLS	KTCH	ASE	PHAR R = MAR2	8 = SAR HR21 BFX1 TF RDC	WHEN RUC THEN 0	JUHP							
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X TRANSFER HIS TO TO THE STANDING TO TRANSFER BENIED TO AZ			A SEND B TO THE ADDER	A JUMP TO FAGING ROUTINE			A TEST IF BREAKPOINT SELECTED	SKIP			# MAR2 CONTAINS ADDRESS		PESTORE	A PERFORM WRITE INTO MEMORY		% CLEAR LC1				A THIS ROUTINE WILL FEICH AN INSTRUCTION		A PRESELECTED VIA A TRACE CUNINGL CARD	A STURE RETURN ADDRESS		- CO - IV	S SR II 2 TO THE ADDER			X ISOLATE ADDRESS IN PAR FIFLD OF FSW				4	A RETRIEVE INSTRUCTION AT ADDRESS IN BF2		A ISULAIE FAR INIO AZ		% TEST FOR UPPER MEMORY BOUNDRY		= A11 JUMP & NCRMAL INCREMENT		% CREATE 1024 IN B				CLEAR PAR	% RESTORE B AND SET PAR TO 1024			S THIS ROUTINE WILL CALCULATE AN ACTUAL		RF G.
_ <	A1 R = 8	SAR SAR	B TE IST THEN STEP ELSE	1 = MPCR	AIR = B	21 = SAR		IF LST THEN STEP ELSE	BKICHP - 1 = MPCR	ASE	BHAR R = MAR2	8 ≈ SAR	A2 = MIR	MW21 IF SAI	WHEN SAI THEN CI STEP	IF LC1	June					A MD CD - A D	ATT CR = AZ	CIATUS - 111	CINDIT - 4 - COCB	B	IF HST THEN STEP ELSE	= CPCR	A1 L = B	COMP 16 = SAR		8 L = 8R2	œ	ENOLIN = 1 = CPCR	AZ = ARPCK	A1 L = A2	A2 R = A2		A2 GTR C	THEN A1 + 1	B = M1R		۵		16 = SAR		A1 OR B = A1, BMI	JUHP				
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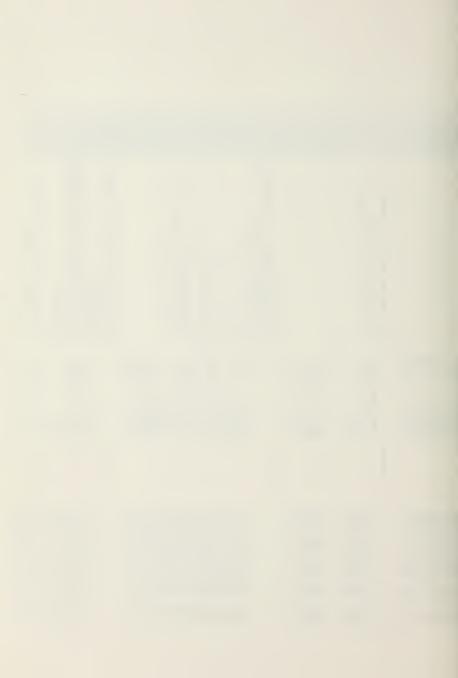
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R GENERATE 512 IN B		M B NOW CONTAINS 768 (ADDR OF PAGEREG)	COO LONGO	A REFERENCE DAZ		T PHI BROKPAGE ANDR DEC MO. N. IN MADO	THE COURT OF THE PARTY OF THE P	S SAVE A2 IN PIR	USE A2 AS X = CELECT MOTORS COS DAAD			DESTREE THE AUDIESS RESISTER	DEAD COMPENS OF PAGE AUDIO MEG.	CAVE DAVE ADEDICE DES CONTENTS OF AD	STATE TAGE ABOUTEST REG CONTENTS IN AZ	A SEL FAGE MUDIFICATION BIT (BIT 15)	STEP FISE SKIP & STORE TO PEHODY, SET	9	FORM PAGE ADDRESS REG PLUS HOD. PIT		MODIFIED PAGE ADDR. REG. IN HIR	A WRITE OUT MODIFIED PAGE REG			MASK OFF LOWER 8 BITS	RESIDNE AZ	B HAS THE PAGE REG. CONTENTS		P E ID CALLING ROLLTING				× 1	2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	*****	A THIS ROUTINE WILL FETCH AN INSTRUCTION (ANALYZE THE OPCODE(UPPER & ETTS) AND	G ROUTINE FOR	KALIUN.	AI TO THE ADDER	A EXPRINE KEPUIE EXECUIE BII	R GET THE NEXT INSTRUCTION				PLACE THE 6 OPCODE BITS IN LOW ORDER 6 BITS OF A2	CREATE ADDRESS OF OPERATION ROUTINE EX	BASE ADDRESS OF OPTABLE	DETABLE BASE		~.	- SEGGES SNEETSHEETS AT SKING FOR BY	POND TO EUPROUTINE CALLS TO THE
8 - 1 -		0 = 1 + B + 1 = B	23 ± L11	CTO - C CHAN TON		EMAR R = HAR2	040 11 74	- 11	BMAR = A2			200 31 400 11	NHEN BOY THEN BOY		0 - 0 000	8 = 8 00E	1C1 THEN SET LC11		A2 OR B = A2	A2 = MIR,BHI		MW21 IF SAI	WHEN SAI THEN O	A2 AND LII = A2	255 = LII	1	CTD 00 B C = BB3		F LC1 THEN SET I C11		PAGEIN - 1 = MPCR			00330 * * * * * * * * * * * *		0P C 0 D E 1			:	TO THE STATE OF TH	RESTPSW - 1 = CPCR	IFEICH - 1 = CPCR	IF LC1	IF LC2	N N N	24 H H H	+	OPTABLE - 1 = AMPCR	TEP	EXEC		OPTABLE:	
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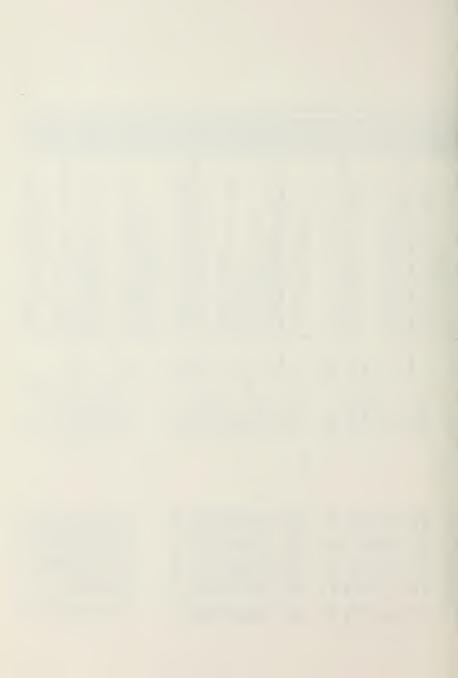
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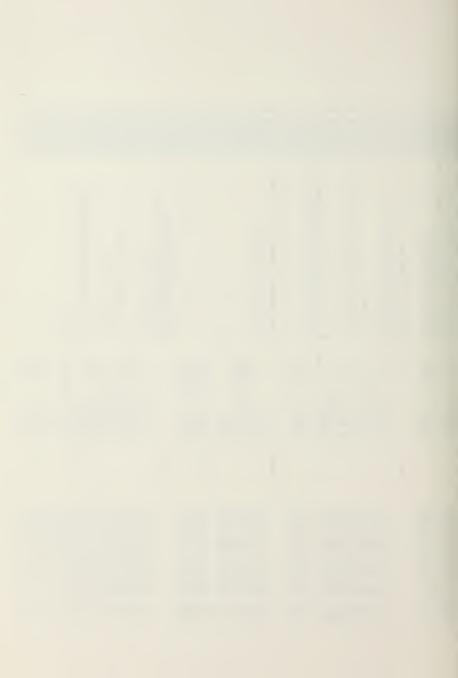
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												THIS DOUBTINE AMAINTES OF OBSESSE	THE PROPERTY OF THE PROPERTY O	F INTO AZ	JUMP TO DESIRED SUBFUNCTION														KX ITPE BY IE		OF Y INTO BITS C-7 OF R(A), AND CLEARS C2426COO	S THE REMAINING BITS OF READ	SET FLAG FOR BYTE INST.				A ADDR. OF Y IN BR2		ELSE SKIP & MS BYTE OF (Y)	# OR LS BYTE OF (Y)		& NEW CONTENTS OR READ	A ARTHMETIC CC SETTING CENTER KITH 9)														ADDR OF DESIRED SUBFUNCTION OF OPCODE	SET UP BASE ADDR OF TYPE OF THSTRUCTION02451000	C1 IS DETERMINED BY ADDING THE FUNCTION02452000	FIELD COUE.			THIS ROUTINE JUMPS TO THE APPROPRIATE	SUBFUNCTION FOR OPCODE C1
- 1 =	# T	- 1 =		11	-	OPC00E74 - 1 = MPCR	OPCODE75 - 1 = MPCR	0PC00E76 - 1 = MPCR		•					A2 + AMPCR = AMPCR &	OPOCF - 1 = AMPCR &	SILP					NOTIMP - 1 = MPCR	FAULT - 1 = MPCR	FAULT - 1 = MPCR	0P003 - 1 = MPCR			•		•	~		SET LC2	0707 - 1 - 0	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		OHP 8 = SAR		C2 THEN STEP	B R = B	8 = SAR1 255 = LIT	AND B = B.MIE				IT AND C - D	CIT AND G = C	REGSTACK - 1 = CFCK	EDUINOI - 1 = CPCR	0PC00E - 1 = MPCR				*	*	XFCODE - 1 = CPCR *	A2 + AMPCR = AMPCR &	OPDIF - 1 = AMPCE &	STEP	EXEC			OPO10 - 1 = MPCR &	UPO11 - 1 = FPCR x
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			SELECT LS 4 PITS OF B ("F" FIELD)		SELECT REGISTER STACK TO DE USED ADDR OF GEN REG STACK RETURNED IN HARZ	PUT CONTINTS OF RCM) IN B	CONTENTS OF PCH) IN HIR	ARTHHETIC CC SETTING (ENIER KITH B)				ADDR OF CEN DEC STACK DETURNED IN MAD	CONTENTS OF PCH 1NTO			200				ADDR OF GEN REG STACK RETURNED IN MARZ	SET UP ADDRESS OF YM IN ERS		READ (Y*) INTO B	(Y*) IN HIR	ARTHHETIC CC SETTING CENTER WITH B)	EXTRACT "A" FIFLD				WRITE OUT CONTENTS OF Y* INTO R(A)			RK TYPE INSTRUCTION		CET CONTENTS OF 1Y FIELD	PREPARE A3 FOR STORAGE OF 17: FIFTD			CLEAR HIR, BR2,		A PUT :H: FIELD INIO MAR	A IP THE PIECU	SALF SANALYZE REM) AND RETURN VALUE IN MIR	Y INTO A2				ARTHRELLC CC SELLING CENTER KILH B)
0P012 - 1 = MPCR 0P013 - 1 = MPCR			B AND LIT = B X		REGSTACK - 1 = CPCR X	FINPUT - 1 = CPCR K	B « TER	= CPCR	A 3 A 4 A 4 A 4 A 4 A 4 A 4 A 4 A 4 A 4	4 = SARY 15 = LIT	REGSTACK - 1 = CPCR 9		FOUTPUT - 1 = CPCR R	0PC00E - 1 = MPCR	w 1	*	8 AND LIT = 8		REGSTACK - 1 = CPCR x	or o		SAR	CPCR		SETCCA - 1= CPCR X	A3 K = 8	B AND LIT = B	REGSTACK - 1 = CPCR x		COUTPUT - 1 = CPCR X		•	*	w 1	TEFTCH - 1 = CPCP	A3 L = A3	COMP 16 = SAR1 15 = LIT	A3 OR B = A3	2	A3 R = A2	= MAR2	TOTAL TOTAL CASE CASE CASE	RM - 1 = CPCK	L = A2	COMP 16 = SAR		A2 + B= 6,41R x	SELUCA - 1= CPCR X
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a re offer a state of the state	to the tieft in to 4 mile of			K (R(H)) + (Y) INTO R(A)	× 01-100-100				A ANALTZE "H" FIELD CONTENTS	K ISOLATE Y INTO BR2		A CTU LAID B	SIORE CT. INIO HIR			0 1010 101 1001	٠,	A ADDR OF GEN PEG STACK RETURNED IN MAR?					A THIS ROUTINE DECODES THE 02 OPCODE		A CLEARS LOCAL CONC. BITS					BC BC						.M. CICLO COLCOTO HAND	S ISOLATE : As FIFTIN				8 8 = (R(A)); FAR2 = RA		ISULATE SHE FIELD		TEST COD NOT IMPLEMENTED BOLLINGS	2	SKIP						
4 4 8 2 8	20 = SAR1 15 = LIT	LIT AND B = 0	REGSTACK - 1 = CPCR	OPCODE - 1 × CPCR	*		0P013:		HAMPIELU = 1 = CPCR	E L = BR2		CFCR		A T D T D T T C T C R	I T CAD AR T TE				EDUTPUT - 1 = CPCR	0PC00E - 1 = MPCR			01.001.021		9000	A) + AMPCD = AMPCD		STEP	EXEC		0P02F: 0P020 - 1 = hPCR	0P021 - 1 =	-	=					LIT AND B = B		 	A3 AND LIT = A2		ODGOOM - 4 - AMDED	= ANFOR		IF IRUE THEN STEP FLSF		EXEC		" "	" ,	
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# IF (G(A)) >= 0 (F(A))+(R(A+1))15 -> FA
# IF (R(A)) <= C (R(A))-(R(A+1))15 -> RA
                                                                                    # IF (R(A)) < C, (R(A)); -> PA
# IF (R(A)) => 0, (R(A)) UNCHANGE
                                                                                                                                                                                                                                                          # IF (R(A)) > C, (R(A)): -> RA
# IF (R(A)) <= 9, (R(A)) UNCHANGE
                                                                                                                                                                                                                                                                                                                                                                  K(R(A)): -> RA ONLY IF LC2 IS SET
                                                                                                                                                                                                         K SHIFT (R(A)) TO UHW OF AZ,B
K TEST FOR MAX NEG. NUMBER
                                                                                                                                                                                                                                                                         R CRCADO INTO UNW OF A2.8
                                                                                                                                                                                                                                                  % TYPE RRI MAKE NEGATIVE
                                                                             A TYPE RRI MAKE POSITIVE
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                                                                                                                                                                                                                                                                                                                                                                                                                                 8 E = (R(A)); HAR2 =
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B = (R(A+1))
                                                                                                                                     SET OR CLEAP OV
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                                                                                                                                                                                  -8 R = 8, MIRJ SET LC2
IF AOV THEN SET LC1 % CHECK FOR CARRY
                                                                                                                                                                                                                                                                                         R A2 TO THE ADDER
                                                                                                                                                                                                                                                                                                                                        IF ADV THEN SET LC1 R CHECK FOR CARRY
                                                                                                                                                                   IF NOT HST THEN STEP ELSE SKIP
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                                                                                                                                                                                                                                                                                                                                                        IF LC2 THEN STEP ELSE SKIP
                                                                                                                                                                                                                                                                                                                                                                                                                                       COMP 16 = SAR 1 1 = LIT
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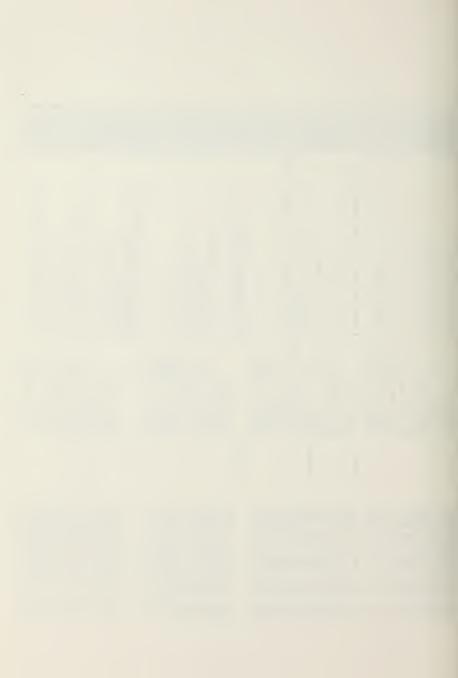
1 F TRUE THEN SET LC 1

0 VB 1 T - 1 = CPCR

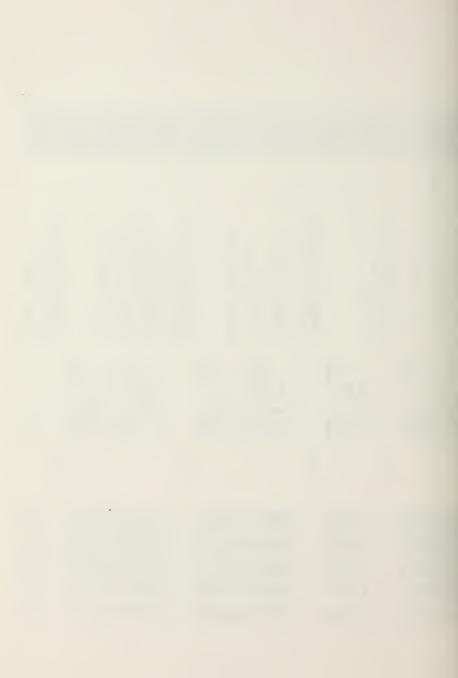
S T E P
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EINPUT - 1 = CPCR
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OPCODE - 1 = MPCR
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COMP 16 = SAP
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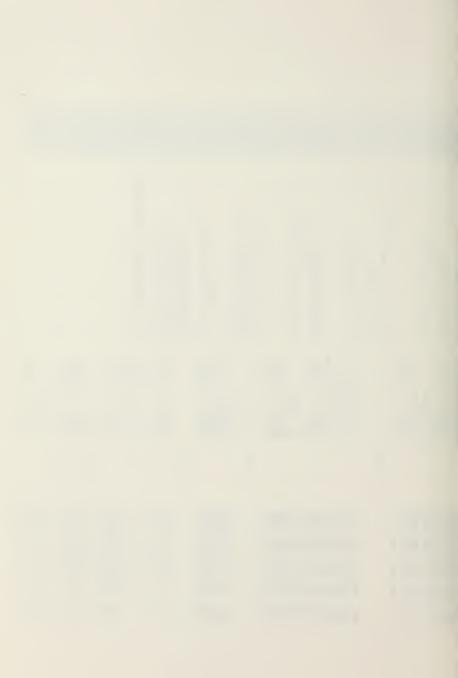
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	CO-FA G THEN TO THE COMPANY OF THE C	# 150LATE 617 15 IN D		CLEAN OUT B REGISTER		PLACE BIT 15 IN BIT 16			CHECK FOR CARRY		OVERFLOW CHECK				OIL TAR IS OF THE INTE		2000	MEUN FUN CANNT		CHECK FOR DVERFLOW	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	SEL OF RIAD INTO HARE	A FURT KA						ST COMPLEMENT: TYPE DO		A AZIB MAYE (KCAJ) IN UHWI MAKZ = KA		UPPK FOD HAY NEG. MITH.	SET /CLEAR DVELT		TWO :S COMPLEMENT (R(A))	CHECK FOR CARRY		1 = (R(A))				TWO:S COMPLENENT DOUBLE; TYPE RR	(RAPEA+1): -> RAPRA+1	REF RR2	TEMP STORAGE OF R(A)		1 = (R(A)); FAR2 = RA		R(A+1)	B = (R(A+1)) HAR2 = RA + 1	A2 = (RA,RA+1)		R TEST FOR MAX NEG NUM		TWO:S COMPLEMENT OF (R(A),R(A+1))	CHECK FOR CARRY	
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RPOS - 1 = MPCR		B × B	S	8 L = 8	COMP 31 = SAR	B R = B	15 = SAR	A2 - B = MIRs SET LC2	IF ADV THEN SET LC1	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR	FND02002 - 1 = MPCR		9 1	,	C	TE ADV THEN COT 1 CA	CADOX 4 - COCO	CARRI - I = CFCR	CHECKUV - 1 = CPUK	C 4 1 0 4 2 0 0		A C ANU BILU = HAKE, U	040 - 74	CETTOA - 4 - CPOR	COUTDIT - 4 - CPCB	TO LOCAL TO	Urculle = 1 = arck	0.48	0.54 + 1 0		A 5 501 8100	IF TRUE THEN SET ICA	0VB17 - 1 = CPCR	16 = SAR	- B R = B.HIR	IF ADV THEN SET LC1	CARRY - 1 = CPCR	SETCCA - 1 = CPCR	EDUTPUT - 1 = CPCR	0PC00E - 1 = MPCR		15:		ASE	BHAR L = BR1	COMP 8 = SAR	R L = A2	COMP 16 = SAR ; 1 = L1T	LIT OR PHAR = HAP2	FINPUT - 1 = CPCR	A2 OR 6 = A2, B	A2 E0L 8100	IF TRUE THEN SET LC1	0VB11 - 1 = CPCR	8 1 8 1	IF ADV THEN SET LC1	CARRY - 1 = CPCR
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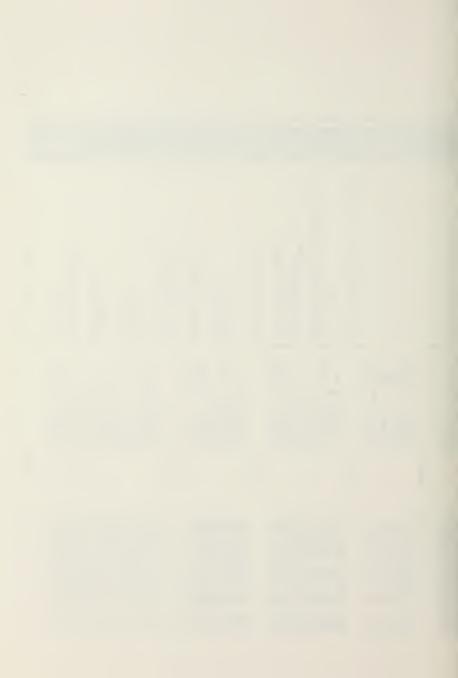
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B. L. # AS BUCKAIT INTERACTOR	SAR		FOUTPUT - 1 = CPCR	S CRCADO INTO MIR	UELE WORD ARTTH COMPARE		22	K B CONTAILS (R(A), P(A+1))			2E	2 ×	8 B = (R(A)); MAR2 = RA		A.A.		9767							•	C4 20 UUI WE VEALURE	TO THE METHOD AND THE PART AND		SET LC1 % CHECK FOR CARRY		CHECKOV - 1 = CPCR & CHECK FOR DVERFLOW -		PIR RESULT IN LHW OF B.MIR				0PC00E - 1 = MPCR		S DECREMENT RA BY 11 TYPE FR	40		P 16 = SAR (R(A)) IN UHW OF A2	LC2 & DECREMENT VALUE IN BIT 16		.C1 % CHECK IF CARRY GFNERATED		CKOV - 1 = CPCR & CHECK IF OV GENERATED		HIR S RESULT INTO LHW OF BUNIN				טרכטטצ - ז = מרכא	88			6 L = A2	
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	000	0 2	0.5	0.2	050	2 5	020	0	0	2 6		0	0 2	0.2	0.5	0.5	0.5	62	2 0	2 0	0 0	0 0	0.0	6.2	0.0	6.5	0.5	0.5	0 5	20	0 0	0.5	0.5	0.5	0.5	0 5	0 2	0.5	02	0.5	0.5	000		20	C 2	0.5	0.5	62	20	0 20	62	20
		R CHECK FOR CARRY		A CHECK FOR OVERFLOW	0.14.0 00 0.14.1					C DECREASE RA PY TWO. TYPE RR	(RA) - 2 -> RA	K B = (RA); HAR2 = RA		(R(A)) IN UHW OF A2	2 % LC2 IS SURTRACTION FLAG			S SET/CLEAR CARRY 611		STRUCK OF STRUCK THIS						A LOAD DOUFLET TYPE RICIL)	R(Ym,Ym + 1) -> RA,RA+1; SFT CC	K ISOLATE :M: FIELO		٥	THE CALL LAND DOUGLE DOUGLE			S LOAD DOUELE, TYPE RX			CALL LUAD DUUBLE ROUTINE		THIS ROUTINE ANALYZES THE 03 OPCODE													
				*	•	•			•	. 14	~	-		L178	_			× ×			•				PK	BK.	get.	p4			4 6	•	SK.	×				×	er.					٠	•							
LIT L = B	A2 + B = MIR	IF ADV THEN SET LC1	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR	BMI B R = B.MIR	16 = SAR	SETCCA - 1 = CPCP	EDUTPUT - 1 = CPCR	OPCODE - 1 = MPCR				B L = A2	COMP 16 = SAR1 2 =	1 10	A2 - 8 = HIR	IF ADV THEN SET LC1	CHECKOV - 1 = CPCR	BHI	P R = B.HIR	16 = SAR	SFICCA - 1 = CPCR		0PC00E - 1 = MPCR				B AND LIT = B		FEBSIALS - 1 = CPUN	LOBIE - 1 - CPCP	0PC00E - 1 = MPCR				RXHFIELO - 1 = CPCR	OPCONF - 1 = UPCR		40	XFC00E - 1 = CPCR	A2 + AMPCR = AMPCR	OFUSE - 1 = ANPER		2 4 5 5	0P030 - 1 = HPCR	1 1	-	н		15 = LIT	A2 + AMPCR = AMPCR	OFUSUR = 1 = ARFCR
										0P029131																11								3:					0PC00E031	-					: 4				: 0			
										0 P 0 2																0P021:								0P0231					OPCC						0P03F:				0 P 0 3 0			
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0 90 O	0 0 E O	0 0 E 0	0900	0900	0000	0050	0900	0900	0 0 4 0				C 0 F 0	COAO	0 OF 0	0.00	0 0 E O	0000	0000	0 0 0 0	0000	0 9 0 0	0900	0046				0 0 F 0	0000	0 9 0 0	0 9 0 0	0040				0 90 0	040			0900	00FC	0000	0 0 0 0		0040	0040	0040	0 10	0	0.050	00FC	200
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0766	0707	0768	0709	07CA	0769	0700	CZCE	07CF	6700				0701	0702	0703	0704	6705	6706	0708	6709	070A	0708	0700	0070				070E	0/01	07F1	07F2	07E3				0756	07E6			07E7	0768	07FA	07FR	,	OZEC	07E0	07EE	07EF	0770	07F1	07F2	



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		EL CE CKIP	* INSTRUCTION NOT IMPLEMENTED		₩	*										* EACLOINE REIGHN OF J = 7 HAL HALI		C B = 1 A z FreeD	S DA = MARO						X STOP MACHINE EXECUTION			SIUNE CORTI INIU				X (SR1) INTO MI9			A SIURE (SKI) INIU KA	•	E STORE (Sp3) INTO RA				X RA = MAR2		A HA INTO AZ		C 25.5 II CI 56	# ISOLATE UYK2C SR2			% TRANSFER RA INTO MAR2		X (SR2) INTO RA			\$ LOAD P; (R(A)) INTO P	
	A 2 0 E U L 1 1	SIFP	NOTTHP - 1 = MPCR	•				-		0P03002 - 1 = MPCR	OPOXOGU - 1 = MPCB		ı	UP03006 - 1 = HPCR		8 = 0 2 4	N 7 CAD: 45 - 111	AND B =	REGSTACK - 1 = CPCR	A1 + 1 L = 8	COMP 16 = SAR	B R = B, MIR	_	EDUTPUT - 1 = CPCR	STOPTIME - 1 = MPCR			AS R = AS	4 = SARJ 15 = LIT			A1 R = B, MIR	16 = SAR	<u>"</u> .	DOCUMENT - 1 = CPCR			A3 R = A3	4 = SARI 15 = LIT	A3 AND LIT = B	REGSTACK - 1 = CPCR	ASE	BIAK = AZ	SIATUS2 = 111	EINPUT - 1 = CPCR	9 1 9	COMP 16 = SAR	BR = MIR	A2 = MAR2	EICCA - 1 =	OUTPUT - 1	OPCODE - 1 = MPCR			
							0P030H1								.0001000	100000											. 1001000	10000									00030021																	0P03004:	
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	0756	0756	0757	07F8				07F9	07FA	07FB	0750	2110	7/15	11/0		0800	0 0 0	0000	C P 0.3	0804	0805	90 30	0807	0 6 0 8	6083			n 8 0 A	0 8 0 8	CROC	0 6 0 0	0 6 0 E	080	CR 10	0812	2700		0 6 13	0814	C815	0616	081/	0 7 0 0	CETA	0818	r81C	0810	081E	C8 1F	0850	0821	0622			



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		R RA IN MARZ	X B = (R(A))			% ZERO PAR	S (R(A)) INTO P UPPER 16 BITS UNTOUCHED	•	* 1		K LOAD SR1 ; (R(A)) INTO SK1				R RA IN MAR2				% CREATE BIT MASK FOR LOADER TOGGLES	SAR	M LOWER MASK OF SRI	SAR	S CREATE MASK ONES IN UHW OF B	K MASK FOR (RA)		M MASK FOR A1 (PSW)	% MASK OFF SAVED PART OF A1 INTO A2	CREATE NE	K CLEAR UHW DF A1		A DESTORE AL			S LOAD SR24 (R(A)) INTO SR2				X PA = MAR2	# P = (R(A))	S(R(A)) = A2				A ISULATE UPPER 16 BITS OF STATUS 2			M NEW STATUS CREATED	K (R(A)) INTO STATUS2				LUAU HULIIPLE, ITPE KX	# D =	00		A STORE Y IN UHW OF A3	
4 = SAR1 15 = LIT	A3 AND LIT = B	REGSTACK - 1 = CPCR	EINPUT - 1 = CPCK			A1 L = A1	ALOR B = Al	1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -			01030051	A3 R = A3	4 = SARI 15 = LIT	A3 AND LIT = B	REGSTACK - 1 = CPCR	EINPUT - 1 = CPCR	B L = HIR	COMP 16 = SAR	LIT L = A2	0 HP 29 =	LIT L = B	112 = LITI COMP 16 =	A2 OR 8 = B	NOT B = A2, BHI	A2 AND B = MIR	NOT A2 = B	A1 AND B = A2, BHI	A2 OR B = B	A1 L = A1	COMP 16 = SAR	A1 K = A1	OPCODE - 1 - MPCE		0P03006:	A3 R = A3	4 = SARJ 15 = LIT	A3 AND LIT = B	REGSTACK - 1 = CFCR	EINPUT - 1 = CPCR	B = A2	LIT = MAR2	STATUS2 = LIT	EINPUL = 1 = CPCR	B = B	16 = 5AK	0 - 7 0	NID = 8 NO 24	EDUIPUI - 1 = CPCR	- T - 100				2000 - 4 - 10000		= SABI 15		
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			16					JATER = C			KA				KIGHT JUSTIFIED			# 27				INTO MAR2		× 1100000000000000000000000000000000000	CACHENI	~							ANALYZES THE C4 OPCODE										ATES THE 1H: FIELD										
A2 = 1H1 FIELD		R = 1A1 FIFTD	_=		SKIP			K IF M = A THEK COUNTER		CONFORT N - A + 1		SAVE RA IN BRI	1	IN BP2	STORE T IN AST	LOOP RETURNS B		RA INTO P FROM BR1			INCREMENT RA	R COMPUTE NEXT RA	RA + 1 = BR1	DB2 +	1 4 240	DECREMENT COUNTER							THIS ROUTINE	THE PIECE IN									THIS ROUTINE ISOLATES THE					SKIP					
4	1			16 = LIT		+ LIT = A2	¥2			T T T AZI AZE		BHAR L = BRILCSAR &	10 M	= A3.8K2		LAULIN - 1 = CPCH A		BHAR R = B, HAR2 &		EDUTPUT - 1 = CPCR K		= CPCR		CURT G II SAR			E01 0	IF TRUE THEN SKIP	LDHUL - 1 = MPCR	- 1 = MPCR	er i			APPLODE - 1 = CPCR X	DPOUF - 1 = AMPCR		EXEC			 	-			LIT AND B = A2		A2 GEO LIT	4 = LIT	IF TRUE THEN STEP ELSE	FAULT = 1 = RIPCR	OPO4H - 1 = AMPCP		EXEC	*
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THIS ROUTINE CALCULATES THE FOLKA) OSCOSCOOF AUTHORNOOTINE RACTOLATES THE FOLKAR ROOTSOCSCOOF A UNHERR FASSED VIA THE B REGISTER, OSCOGGOOTHE FOUNDER BOOTS BETTER OSCOGGOOTHE FOUNDER BY AZA
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                                                                                                                                                                                                                                                                             ΑY
                                                                                                                                                                                                                                                                                                                                                                           UNUSED
                                                                                                                                                                                                                             X SHIFT NEXT PAIR OF DIGITS INTO
STEP ELSE SKIP
X FINI$HED
                                                                                                                                                                                                                                                              STEP ELSE SKIP
EXAMINE NEXT PAIR OF DIGITS
PARTIAL SORT EFFECTIVELY HULT
                                                                                                                                                                                                  MS PAIR OF DIGITS
                                                                                                                                                                                                                                                                                                                                                      B
                                                                                                                                                                                                                A3 = PREV. REH/NEXT FAIR OF TEMP STORAGE
                                                                                                                                                                                                                                                        CHECK FOR 00 PAIR OF DIGITS
                                                                                                                                                                                                                                                                                                                                                     SKIP & RESTORF REMAINDER INTO 8 % RESTORE REMAINDER INTO 8
                                                                                                                                                                       SET FOR 16 ITERATIONS
                                                                                                                                                                HIR USEN AS TEMP STORAGE
CTR SET FOR 16 ITERATIONS
                                                                                                                                                                                                                                                                                                                                                                           REGUIRED TO PALANCE LAST
                                                                                                                                                                                                                                                                                                                   R BUILD PARTIAL SORT
R PREPARE FOR NEXT DIGIT
                                                                                                                                                                                                                                                                                                                                                                                                     SET THE CONDITION BITS
                                                                                                                                                                                                                                                                                                POTENTIAL REPAINCER
                                                                  SET OV AND CC BITS
                                                                                                                        BR1
                                                                                       ISOLATE "A" FIELD R(A) INTO HAR?
                                                                                                                                                          B = (R(A),R(A+1))
                                                                                                                                             HAR2
                                                                                                                                                   (R(A+1)) INTO 8
                                                                                                                        RCA+1) IN
                                                                                                                                                                                                                                                                                                                                                                                        REMAINDER INTO
                                                                                                                                                                                                                                                                                                              HARZI SET LC11 SKIP
                                                                                                                                             R(A+1) INTO
                                                                                                                                                                                                   FETCH NEXT
                                                                                                                                      R(A+1)
                                                                                                                                                                                                                                                                                                                                       IF NOT LC2 THEN STEP ELSE SKIP
PAIR - 1 = MPCR
                                                                                                                                                                                                                                                               A28
                                                                                                                                                                                                                            COMP 2 = SAR
1F COV THEN SET LC2; S
SEND - 1 = HFCR
COMP 1 = SAR
                                                                                             = CPCR
CPCR
                                                                                                                                            = CPCR
CPCR
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MPCR
MPCR
MPCR
                                                                                5 = LITF q = SAR
IT AND B = B
                                                                                                                                                                                                                                                                                                                                                                                                     CPCR
                                                                                                                                                                                                                                                       A3 EOL 0

1F TRUE THEN A2 L

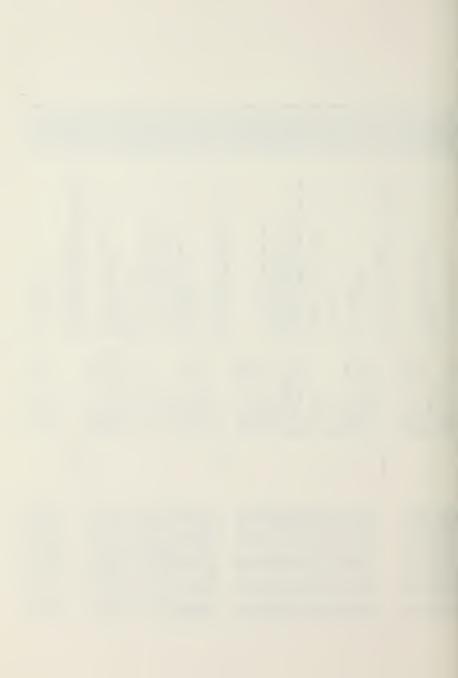
PAIR - 1 = HPCR

A2 L = 8

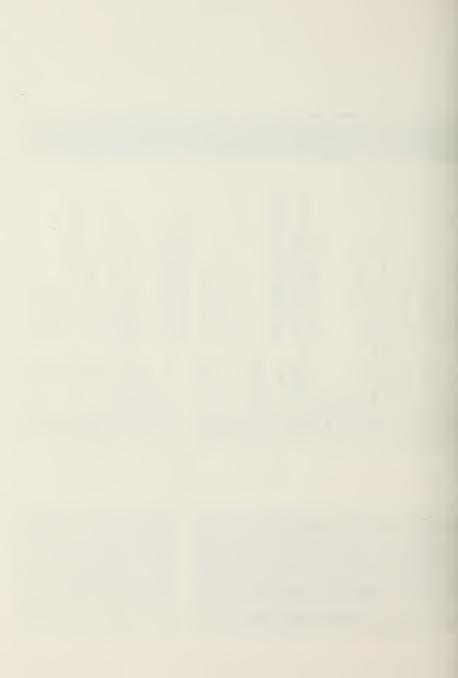
COMP 1 = SAR
                                                                                                                         BR 1
                                                                                                                                                                                                                                                                                                                                                       11
                                                                                                                                                                                                                                                                                         B + 1 = B
A3 - B L = HAR2
COMP 2 = SAR
1F MST THEN A3 L
                                                                                                                                             10
                                                                                                                                                                                                                                                                                                = MAR2
                                                                                                                                                                        .9 = SARF 15 =
                                                                                                                                                                                                                A3 OR BHAR = A3
                                                                                            REGSTACK - 1 = CP
EINPUT - 1 = CP
B L = A2
COMP 16 = SAR
                                                                                                                                                                                                                                                                                                                                                    IF LC1 THEN A3
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A HOVE (R(A)) RIGHT 1 BIT
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B = (R(A+1))
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B = (R(H))
HIR = (R(H)) + 1
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                                                                                                                                                                                                                               EDUTPUT - 1 = CPCR
SETCCA - 1 = CPCR
1F LC2 THEN STEP ELSE
OPCODE - 1 = MPCR
                                                                                                                            BHAR + 1 = HAR?, hIR
IF NOT COV THEN INC
                                                                                                                                                 A3 + LIT = B
REGSTACK - 1 = CFCR
EQUIPUT - 1 = CPCR
PPCORE - 1 = MPCR
                     CPCR
                                                                                                                                                                              SET LC2
RXHFIELD - 1 = CPCR
                                                                                                                                                                                                EMULIN - 1 = CPCP
8 = SAR; 255 = LIT
1F LC2 THEN LIT AND
                                                                                                                                                                                                                      REGSTACK - 1 = CPCR
                                                                                                                                                                                                                                                     REGSTACK - 1 = CPCR
EINPUT - 1 = CPCR
                                               IF NOT ABT THEN AZ
                                                                                                                                                                                                                AEOM - 1 = CFCR
                                                                                                                                                                                                                                                                  - 1 = CPCR
                                                                              LCTR; SAVE
A2 AND B R = A3
30 = SAR; 3 = LIT
                                      # A21 ASE
                                                                                                                                              = SAR; 2 = LIT
3 + LIT = B
                    REGSIACK - 1 =
CINPUT - 1 = CP
       BHAR L = BR1
COMP B = SAR
DMAR + 1 = B
B L = A21 ASE
COMP 16 = SAR
                                                                                                                                                                                                                                                                        - 1
                                                                                                                        1 = SAR
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COMP B = SAR
                                                                                                                                          = A3
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A2 L = A2
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A2 OR D =
A2
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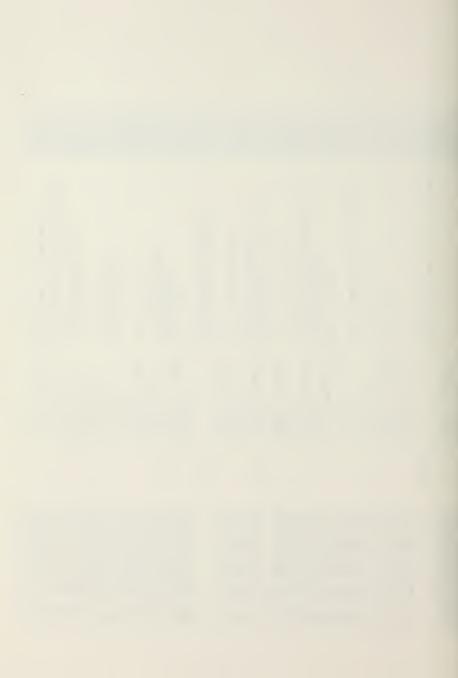
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	S THIS BOILTING ANALYZES THE OR OPCODE	THE WAY I TEST INC							•							S SBR SFT BIT 1 -> (R(A)))			X B = tAt FIELD		4		% B = (R(A))			X 8 = tMt FIELD		S VARIABLE SHIET AMOUNT FOR LEFT SHIET		Market A Third A Co. Co.	A SEL I INIO UNIO SIONE INIO DIN	HODIFIED CREADS ->			54	K IVII IDAD AND INDEX BY 4.5	1405 01401			א פ יייו דוברו		\$ (R(H)) = Y* = B	_			2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2			s	S RA = HAR2	8 (Y) OR (Y+) -> RA		K (Y) OR (YW) -> P	SKIP					K H = (R(H))	% HIR = (R(H)) + 1				2	A LXJ LOAD AND INDEX BY 1	% TYPE RX	% B : ≺	S LOAD AND INDEX BY 1	
	OPCOOF 05 1	VECODE - 1 - COCO		A2 + AMPCR = AMPCR	0P05F - 1 = AMPCR	STEP	FKFC	,	6	4	-	10	-	•		000501	0	1	4 = SAR1 15 = L11				FINPUT - 1 = CPCR			AS AND LIT = B	15 = L17	1 B = SAR	8001 t = 8	a. a. H. a. a. c. 4	01 VIII - 0 VO 2V	EUUIPUI - 1 = CPCH	SETCCA - 1 = CPCR	0PC00E - 1 = MPCR		0 0 0 5 1 1		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0				EINPUT - 1 = CPCR		LD1NX1: B L = 8R2			2 - 1 - C - C - C - C - C - C - C - C - C	¥	11	REGSTACK - 1 = CPCR	EDUTPUT - 1 = CPCR	BHI	SEICCA - 1 = CPCR	IF LC2 THEN STEP ELSE	DPCORE - 1 HPCB		0 1 0 0	REGSTACK - 1 = CPCR	FINPUT - 1 = CPCR	R + 1 = H1R	EDUTPUT - 1 = CPCR	OPPOSE - 1 MODE	10000		01 0531		- 1	LOINXI - I = MPCP	
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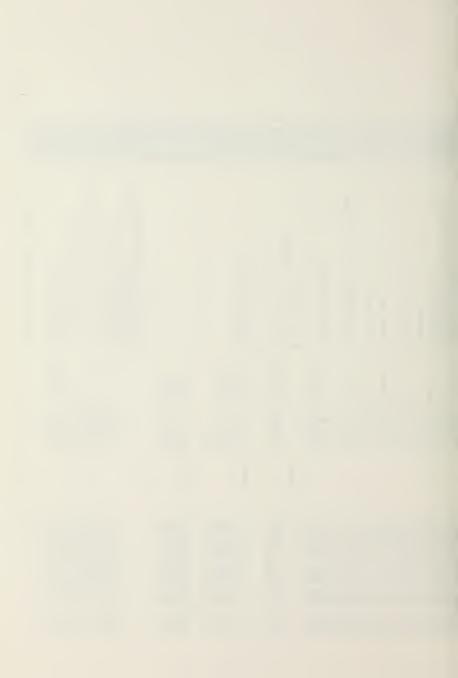
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A THE AUDITME SHALLES THE UE STUDIES										100 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0			,	% B = :A: FIELD		X P = (R(A))		X B = :M: FIELD		% VARIABLE SHIFT ANOUNT FOR RIGHT SHIFT		M MASK	C -> (R(A))H	K HODIFIED (R(A)) -> RA			A LUXII LUAD DUUBLE (INDIRECT)	A INDEA DI 1407 HILES			8 5 = (R(M)) = Ya		~			SKIP X : A: = : H:		% RM = MAR2	% B = (R(H))			(- / + ((m)))			X TYPE RX	Y 11 12 18	X LOAD DOUGLE	M INDEX BY TWO	•		% THIS ROUTINE ANALYZES THE CZ OPCODE					
XFC00E - 1 = CPCR	AZ + AMPCR = AMPCR	CTCB - 1 = ANFCR	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2					1		00000		9 2 2 3	d=SARJ IS=LII	LII AND B = F	REGSTACK - 1 = CPCR	EINPUT - 1 = CPCR		. A3 AND LIT = 9	15 = LIT	LIT - B = SAR	32 = LIT	#110 C = B	AZ AND B = BIRAB	FOULD = 1 = CPCR	UPCUDE - 1 = HPCH		01.001.0	LIT AND B = B			EINPUT - 1 = CPCR			LDINX2: AEOM - 1 = CPCR	A2 = B	IF LC2 THEN STEP ELSE	0PC0DE - 1 = MPCK	REGSTACK - 1 = CPCR	FINPUT - 1 = CPCR	C11 + B = AJK	CONTRIL - 4 - CBCD	0PC00F - 1 = CPCR	•	0P063:		RXMFIELD - 1 = CFCR	138LE - 1 = CPCR	LDINX2 - 1 = MPCR			0 P C 0 D E 0 7 t	XFCODE - 1 = CPCR	A2 + AMPCR = AMPCR	CTCD		3 3 7 7 3
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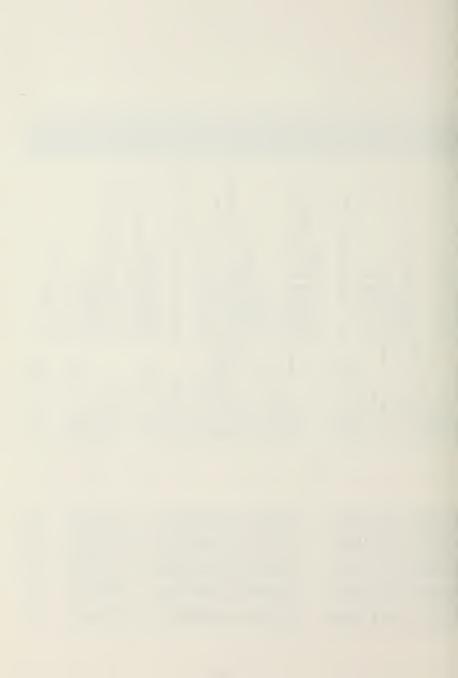
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	2 4	FOR	OF F	CREATE NEW AS VALUE FROM CRCAD)	R CLEAR UHW OF A1			HEXT SEG Y OR Y.			(Y**2) OR (Y*2) = B		SKZ = MAKZ	(CIAIICS)	ISOLATE UPPER 14 RITS OF STAINS			CREATE NEW STATUS?			K LPs LOAD PSW	(Y,Y+1,Y+2) -> P,SR1,SR2	₽ = ⊀			LOGICAL RIGHT SHIFT												KK TTPE LUGICAL KIGHI SHIFT SHIFT (R(A)) RIGHT BY THF IS 5 BITS	FILL, ANT SET C	# (R(H)) INTO 8	A MIN USEU AS LEAP FUR (NCD)	TA SO COOL SE IN TO SO STATE CONTRACTOR	5	SAR HOLDS PITS 0-5 OF (R(H))		SET CONDITION BITS	WRITE WEW (R(A))			RK TYPE LOGICAL RIGHT SIRGLE SHIFT
NOT D - A T . D M	S S S S S S S S S S S S S S S S S S S	•	8 = A3, BHI K	84 B		COMP 16 % SAK			A2 L = BR2	4	- 1 = CPCR ×	•	* MARZ = 111	a D d J			B L = B	= H1R x	EDUTPUI - 1 = CPCR	UPCUDE - 1 = NFCR	, se	set.	RXMFIELD - 1 = CPCR & B	= MPCR	et s	et set	XFCODE - 1 = CPCR X	= AMPCR	0P10F - 1 = AMPCR	SEP		: set	- 1 -			,	get i	T W		CONTENTSRM - 1 = CPCR & C		1901 - 4 - 6050	1011	~		ut.	Z Z	OPCODE - 1 = MPCK	**	HZ.
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nane eran	UADS FCS 6	4809 Enn 2 0830	4809 ACS 6 100C	4809 ECSC 987r	4009 A001 4000		4809 ACSC 4000	4809 CCC 0 2030	4869 COUI OCIO	0000 0000 0000	1 50EO 0800 GCOR 006	4809 5059 5086	0220 000 0000	2F3C 00C3 0000	4609 0040 6890		4869 0641 0806	4869 CC5C F096	0000 0000 0542				5700 0003 0000	3 4 8 C			0900 0000 0000 3635 !	4869 C640 0030	13FC COCO 000C	4809 0000 0000 0000	200		1400 0000 0000	2000 0000 0000 0000	1420 0000 0000					1380 0003 CC3C 0060	4809 FDC3 0R30	2286 0003 0000	4809 0043 1030	1 4809 0C40 C030 80F0	4809 EDCD 8880	2000 0000 0000	2F50 00C3 000C			
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WITH 0-5 FLACE																	0 % 0	0							FL AG											LSB		INTO						PUT (R(A)) - EITS 0-7 INTO 2NE LS BYTE										0 F													
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CRCA)	9						N .	ER CR	H H	C 1 10N	INTO	INI		N	H SHI		0000	RURI				FFY		9	ED AS	INTO	638			_	10 8	TO HI	SNI		NI C	011	1 N 10	IF LC	E 0F	THE H				3			NIAIN			2 2	L 3 B1			8118	NIAIN	NCF	AE 2	1 N 1	0 0				SHIFT	T 0 A 2			
SHIFT (REA) RIGHT T	Y INTO B		A ISOLATE "M" FIELD				A CK(N)) INIU B	A TRANSFER (R(H)) INTO	Y INTO HIR	INSTRUCTION INTO	(RCA)) INTO B	CREASS INTO AT		TCO-5) INTO SAR	PERFORM SHIFT		L A	SEI AFFRUTAILE CUMULITUR BILS				RX TYPE EYTE STORE		(RIA)) BIIS 0-/ INIO T BITE	LC2 USED AS LYTE OPERATION FLAG	Y ADDR INTO B	YINTO			STORE Y	Y) IN	\$ (Y) INTO HIR	FSTOR		A CK(A)) INTO	K (R(A)) BITS (0-7) INTO 2ND LSB	3	<u>د</u>	A LS BYTE OF Y	S CLEAR THE MS				UT CR	IN A3		HIR CONTAINS NEW CY.)	10E0 AC A 10E	010	CRIMAL OF DAYS OF D	LEAK			(RCA)) BITS C-7 INTO LS EYTE	MIR CONTAINS NEW CYS	REFERENCE ART	Y INTO BE?	THE STATE OF THE S	=				RIGHT SHIFT AND STORE	"F" INTO A2			
94 BK			×			_		*		ы	×				-					×	×	*		•	×	×				se.	×	×			e 1	~	SAR	E SKI	×					et.										×	×					,	pe i			ec ec			
	CPCR					и	# CPCK				= CPCR					CPCR		2 0	# HPCK							= CPCR					CPCR			010	CONTENTS A - 1 = CFCR	LIT AND B L = A3, BHI	255 = LITI COMP 8 = SAR # (Y) INTO B	IF LC2 THEN STEP ELSE SKIP & IF LC2 SET, PUT BYTE INTO	CR					~				0.0	5									0000						PCR	MPCR	P C B	
	н		= 3					=	HIR		A - 1				R, B			: د ا	11									010	SAR	-	1 = C				H .	"	1 COM	EN ST	= PP	CSAR	SAR		-	, CSA			2	1		0100	C 3 A R		CSAR		HIR		0		٠.					1 = C	¥ = 2	H 4	
	CH - 1	HIR	A3 AND LIT	15 = LIT		IF INUE THEN	CONTENISKA -	B = A2, BMI	A2 + B = MIR	Ф	CONTENTSRA -	R = AY. BHI		SAK	A3 R = MIR, B	FOUTPUT - 1 = CPCR		SEICLA - I - CFCR	OFCODE - 1						L C 2	RXHFIELD - 1	R I = AR2	COMP a - CAD	0	= BR1	ENULIN - 1 =	HIR	~	2011	FNISH	AND B	= []	C2 TH	S103 - 1 = MPCR	B I = B. CSAR	COMP 24 = SAR			A3 R = A3, CSAR	8 = SAR	A3 L = A3	3 08 B = HIR	Curtot - + - MPCD	2		T = 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	= SAK	B L = B, CSAR	A3 R = A3	A3 OR B = HIR		FMAR = BR2	CALL THE PERSON		UPCOUE - 1 = APCE				KFCODE - 1 = CPCR	A2 + AMPCR = AMPCR	OP 11E - 1 = AMPCR	
	IFETCH	R = HIR	A S A	1 2	C EOL B		200	# ED -	4 S 4	A 3 = B	CONT	12		H D	A 3 R	FOUT	0 1 1 0	2000	0 7 0						SET LC2	RXHF	-	0 10 0	1000	EMAR	ENUL	B = MIR	A.3 = B	2 0	C ON	=	255	1	L S 1 0	- 6	COMP		¥ .	A 3	8	A 3 L	A 3 0	CMT		0	E 1	11	ب 8	A 3 R	A 3 0	ASR	FHAR	× 1	2000	UPCO				XFCO	A 2 +	0 P 1 1	,
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									R RR TYPE ALG RIGHT SINGLE SHIFT	SHIFT REAL RIGHT CREMIN CO.S.	CICH CITE AND DET OF		K (RCH)) INTO B	TEMP STORAGE	# PUT INSTR BACK INTO B	R (R(A)) INTO B	R CREATY INTO A3. COCMYS INTO D	R PAG. SIGN BIT OF (BAA), 1410 IS BIT			****** *** ** *** *** **** ****	A TENE TOR A NEGO CACAD	N KESTURE AS	A A CUNIAINS (R(N))		% B = 1111/000C		A3	% SAR CONTAINS (RCM)) (0-5)	R PERFORM ALG SHIFT	% CLEAR UHW B		R RESTORE (R(A))	S WRITE NEW (R(A))	& ARTHMETIC CC SETTING (ENTER WITH B)				R RI TYPE 2 STORE. (RIA)) INTO Y.	% CR(A)) INTO B. R(A) INTO MS A3	E TEMP STODAGE OF (D(A))				***				A RK TYPE, ALG, RIGHT SINGLE SHIFT	A SHIFT (R(A)) RIGHT Y (0-5)	K SIGN FILL, AND SET CC					K (R(h)) INTO B			R A3 = (R(P))/INSTRUCTION	# Y INTO B
STEP	EXEC		**	OP111 - 1 =	1	10			0P1101				SRH - 1 = CPCR	B = MIR	A3 = 8	CONTENISRA - 1 = CPCR		0 4 2			LOT TUEN CET 1 C4	EN 351 LC1) ×	A	D = 0			HEN A3 OR B =		A3 R = B		COMP 16 = SAR		24	- 1= CPCR	0PC 00E - 1 = MPCR		•	0P1111	CONTENTSRA - 1 = CPCR		august - Nas	1	0.00	0000				0P112:	-	•	LIT AND B = 6	15 = LIT	8 EQT 0	IF TRUE THEN SKIF	CONTENTSRM - 1 = CPCR K (R(h)) INTO	8 F = B	COMP 16 = SAR	A3 OR R = A3	IFETCH - 1 = CPCR
0.000	COF C		0040	0 0 0 0	0 0 11 0	0 6 0 0							1900	0.000	0 30 0	0900	0.00	a o E o	0100	0 100		0 100	0.100		0.00	000	0050	0.00	80F0	C 0 F 0	C 0 F 0	0 62 0	0 0 E O	0900	3900	0000				0900	000	0.000	0 0 0 0	0.00	0 9 0 0	0.40						0 0 0 0	0 0 E C	0 0 F C	COF0	0900	0 0 E O	0020	0 O E O	3900
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K (H(M)) INIU A2		Y INTO A? .			ISOLATE "A" FIELD	ADDR OF FIRST INIO DARK	A CRIAN INTO B	THE STEE STEEL STE			A3 = 1111/00c0			. >			CLEAR UHW B				SET THE CONDITION BITS				RX TYPE STORE, CRCA) INTO Y		INIO NIE		SHIFT "A" TO LS PILS	0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1										"F" IN A2															ZERO FILL AND SET CC		% ISOLATE "A" FIELE	
l		A2 + B = A2		_	AS AND LIT # B	1 = C C C E	ווייייייייייייייייייייייייייייייייייי			IF LST THEN NOT 0 = A3		0 4 0			~		8 F = 8	~	PR = 8, MIR S	= CPCR	-	0PC00E - 1 = CPCR	w	•		- 1 = CFCR	B L = HIK	G = SAR	A3 K = A3 L = SAR: 15 = 111			CPCR			ULOUT - 1 = CPCR		*			XFC00E - 1 = CPCR 8	A2 + AMPCR = AMPCR	0P12F - 1 = AMPCP	STEE			3	 	H	ı		wit i	et i	* 1	er i	1 CC CC CC		T AND E = B	
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THE THE PART OF THE PART OF THE PARTY OF	(SAVE RCA)	K (R(A)) INTO B			S (RCA+1) INTO B	1 A2 = (R(A))/(R(A+1))	R ISOLATE "H" FIELD		R RCH) INTO MAR2	A CREAT TRIO P		K SET THE CONDITION DATE				R (R(A)) INTO HIR		A WRITE OUT SHIFTER (READ)		K (R(A+1)) INTO MIR	X R(A+1)					A AL LIPE / SIUNE DOUBLE	= CPCR % (R(A)) INTO B, R(A) INTO MS WORD AS	R TEMP STORAGE FOR (R(A))	K (R(M)) INTO B			K (R(A)) INTO Y**	TEMP HOLDER FOR Y* + 1		S R(A+1)					AUDR UP T# + 1					RK TYPE LOGICAL RIGHT DOUBLE SHIFT			. *Y* INTO B		MOTE CHOICE AND COLOR MAN	S ISOLATE "H" FIFLD	
- 1 - cren	COMP O - CAS	I - 1 = CPCR		COMP 16 = SAR; 1 = LIT			9	15 = LIT	= CFCR	D = CAC	P. CET 104			R = HAR?	B = SAR	œ		A2 1 = A2	COMP 16 = SARE 1 = 1 IT	= MIR		EDUTPUT - 1 = CPCR	0PC00E - 1 = MPCR	K		,	CONTENTSRA - 1 = CPCR		M - 1 = CPCR	B L = 6R2		PCR	BUAR + 1 = HIR	15 - 040 - 45 - 124	OR 1 = MAR2	CR	A3	INB	A3 = HIR B 1 = DB2		CUMP 8 = SAK	0PC00F - 1 = MPC8		t se	14	*	*	IFETCH - 1 = CPCR 8		15 = SAN 15 = LII	C	
-																									. 10 4 0 0	017110																			0P122;							
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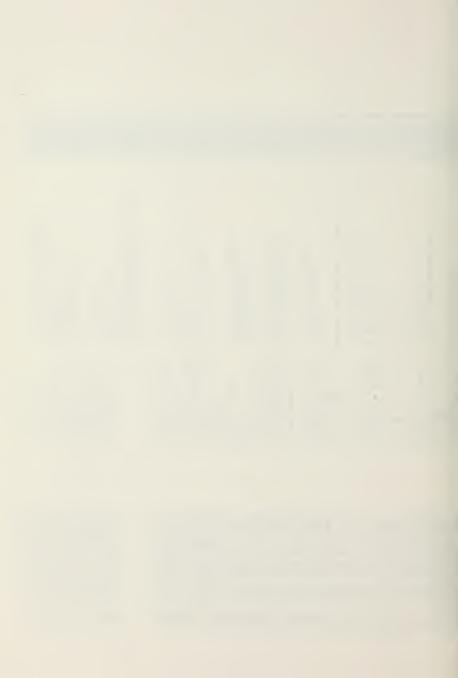
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	STEP	K (R(H)) INTO B	"Y" INTO A2		A TINIU AZ		X ISOLATE "A" FIELD				SAVE ABOR OF READ IN BRI		CREAT INIO DS AS	864413	(R(A+1)) INTO D	D = (R(A))/(P(A+1))			SET THE CONDITION BITS	SHIFTED (R(A)) INTO KIR	DE LE	ADDR OF E(A)		WRITE NEW (RCA))	R(A+1)		ISOLATE (R(A+1))		# WRITE NEW CRCA+1))			K STORF DOUBLE	STORE (R(A)) INTO Y, (R(A+1)) INTO Y+1	A Y INTO 8	& TRANSFER Y TO MIR			X ISOLATE "A" FIELD		ADDR UF K(A) INIU MARZ	CREAT INTO E Y TATO E	SAKE ADDE OF BEAT THE AT	SA NI LAM UP HUNG SANS		WRITE CREAD INTO Y	Y + 1 ADDRESS		_	(3(A+1)) INTO B		ADDR 0F Y + 1			
	N SET LC11	TENISRH - 1 = CPCR	ď		A2 + 6 = A2 A3 R = B	4 B SAR	B = B		K - 1 = CPCR	EINPUT - 1 = CPCR X		G II SAR	16 = A3	0	EINPUT - 1 = CPCR X		A2 = SAR	P R = B, A2; SET LC1 X	SEICCA - 1 = CPCR	AZ K = FIR	IO II OAK	R H HARO		- 1 = CPCR	LIT OR BHAR = MAR2 K	16 = SAR	= A2		COUIPUI - 1 = CPCR	1 - 3001	K 94			RXMFIELD - 1 = CPCR 1		A3 R = A3		= B	6	CAMBER CPCR *		PA II PANE	B 1 = B23	COMP 8 = SAR	EMULDUT - 1 = CPCR X	11 OR BHAR = A2	1 = 1.17	-	EINPUT - 1 = CPCR X		A2 L = BR2	FAILURE - 1 = CPCR	PC00E - 1 =	
																																0P1231																						
COF C	0 00 0	0900	0 0 0 0	0020	0010	3000	0 0 F 0	0 0 E 0	0900	0900	0 100	0000	0 4 0 0	0000	0900	0 0F 0	0 40 a	0 OF 0	0000	0 40 0	200	0000	0 0 1 0	3903	0 0 E 0	0 0 V O	COFC	PCF	0 900					0 9 3 0	0 90 u	0 0 E 0	0000	COFO	ODEC	0 90 0	COFO	COFO	COFO	0030	0900	COFO	0 0 E O	C 0 F 0	0900	COFC	0010	0 9 0 0	0040	
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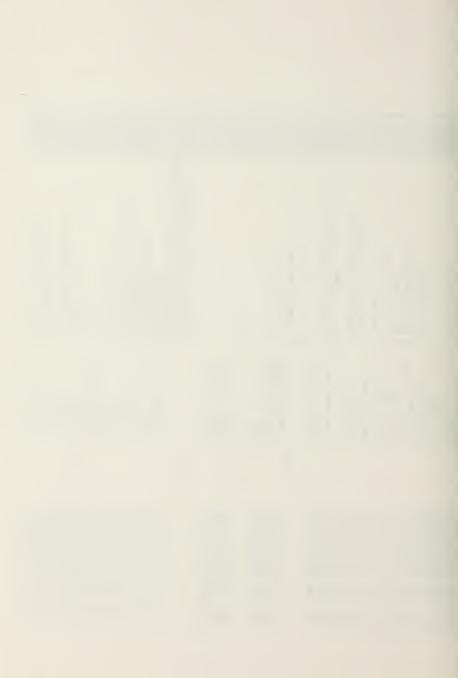
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		EHIFT	"F" INTO A2																RR TYPE ALG RIGHT DOUBLE SHIFT	SHIFT (R(A),R(A+1)) RIGHT R(H) (0-5)					ISOLATE "A" FIFLC	ADDR OF REAL THEO MAD?			TEMP STORAGE OF (R(A))		TEMP STODAGE OF BEAN					A2 = (R(A))/(R(A+1))				ISOLAIE "A"			S (R(M)) INTO P	CRCHOOL COLES INTO CAR	TALL DESCRIPTION OF THE PROPERTY OF THE PROPER	A AZ PAS RIGHT SHIFTED (R(A))/(R(A+1))	SET THE CONDITION BITS	81 SKIP			ADDR OF READ INTO MAR?		COCALL INTO HID			WRITE DUT SHIFTED (R(A))			SHIFTED (R(A+1)) INTO MIE	R(A+1)						PK TYPE ALG RIGHT DOUBLE SHIFT	SHIFT (R(A),R(A+1)) RIGHT Y(0-5)	CIEN ETII AND CET CC		
×	~	×	w					٠		*							•		×	•	*	ŧ			167	*			W?	-	*	t		ВS	sk.	**			1	×			P¢.				×	- 81			84		٠	•		×			**	p¢.			٠	ye.	×	947	Set.	•		
			XFC00E - 1 = CPCR	A2 + AMPCR = AMPCR	OPISE - 1 = AMPCR	CIEP	- C - L - L - L - L - L - L - L - L - L				1 1	FAULT - 1 = MPCR		1										4 = SAKI 15 = L.II	LIT AND B = P	REGSTACK - 1 = CPCR	THOUSE A POOL	THE CLUR	P L = A2	COMP 16 = SAR: 1 = LIT	RMAR I = RR1		COMP 8 = SAR	LIT OR BRAR = MAR2	(INPUT - 1 = CPCR	A2 OR B = A2	4.2	COT LOS MONT LOW OF	IF HSI INEM SEI IUZ	AS AND LII = B	15 = LIT	REGSTACK - 1 = CFCR	EINPUT - 1 = CPCR	B = SAR	20 - 47.00 - 67.1 - 6	AZ K = AZBBI SEI LCI	SEICCA - 1 = CPCR	2 THEN 8111 L	8 = 0	A2 OR B = A21 ASR	BHAR R = MAR2	SAR	A D B = MID	24.2 - 24	200 1 01	FOUTPUL - 1 = CPCR	A2 L = A2	16 = SAR; 1 =	A2 R = HIR, B	LIT OR BHAR = MAR2	FOUTPUT - 1 = CPCR	OPCOL = 4 ~ MPCB							0 1 0 0 0 0	10
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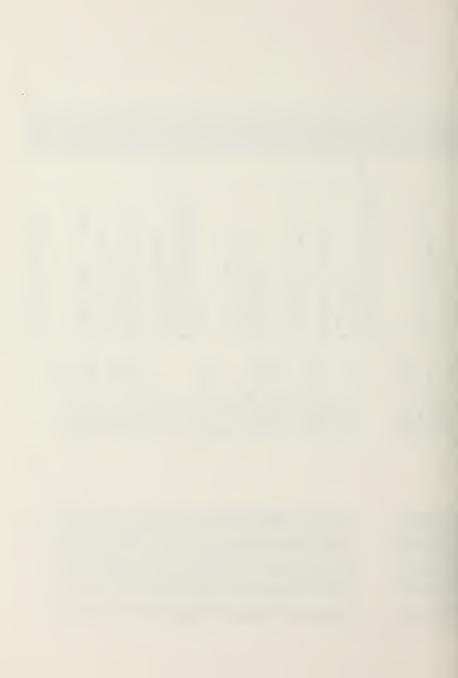
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	י ראברגי - וו - ו מו מ	R (R(H)) INTO B		MAT TOLICE SMILL CHANGE A FEATURE	A TATE OF THE PROPERTY OF THE PARTY OF THE P			X Y INTO AZ	SOLATE *A*	0 0	A ADD OF DAY THE MADE				A SAVE ADDR OF R(A) IN BRI		K CRCA+13 MAIO D	A3 = (R(A)/(R(A T(0-5) INIO SAR					F PEFERENCE BRI				M WRITE OUT NEW (R(A))	D 4 4 10		S HEW (R(A+1))					(R(A), R(K)) INTO Y, Y+H-A+1		SAVE T IN BRI	22						CALCOLATE 16 + (M-A) + 1	A 3 15 NEG CTF, B HOLDS "A"	
1) = (1)		CONTENTERM - 1 = CPCR	R L = B	16 = SAR	CPCR		16 = SAR	A2 + B = A2		A T AND D - D	0.500 =			16 = SAR	= BR1		EINPUT - 1 = CPCR .	1 = A3	A3	HST THEN SET LCZ	A C H SAK	SETCCA - 1 = CPCR X	1F LC2 THEN B111 L = B1		A3 0R B = A3 8	NAME OF THE PERSON NAME OF THE P	8 = SAR	A3 R = HIR		COUTPUT - 1 = CPCR X	LIT OF PRAR = MARS *	A3 L = A3	8	EDUTPUT - 1 = CPCR		. *			IFETCH - 1 = CPCR X	COMP 4 - CAD	AT AND LIT AS	=	A3 R = A3	DNA		IF NOT MST THEN B + 1 =	17 = L17	-8 L = A3, BHI S	COMP 16 = SAR
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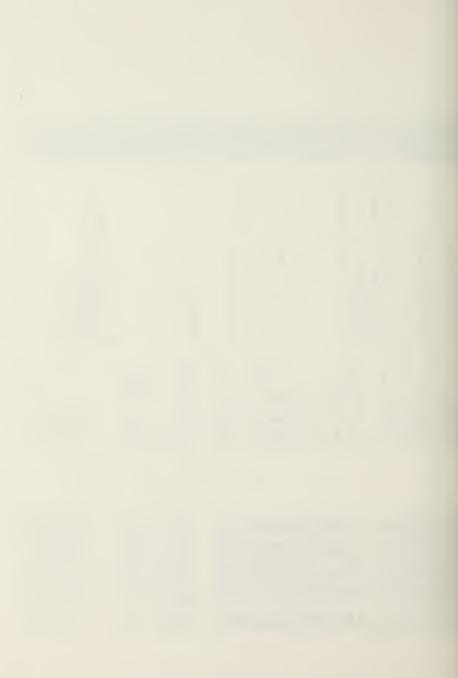
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R (R(A)) INTO MARZ					R A3 = -CIR/R(A+X)		S LOAD BR2 WITH Y	A WRITE OUT NEW Y VALUE	MEXI Y ADDRESS	K SAVE NEXT Y IN BRI		* 1 IN BIT 16 OF B		S INCREMENT NEGATIVE COUNTER	S ISOLATE ADOR OF NEXT R(A+X)		R A3 TO THE ADDER	SKIP & IF CIR NEG, FETCH PEXT R(A+X)	K RETURN TO TOP OF LOOP			•	# ALGEBRAIC LEFT SHIFT	S "F" INTO A2						96						*	R RR TYPE ALG LEFT SHIFT (REGISTER)	& SHIFT (R(A)) LEFT (R(H)) (C-5) PLACES	R ZERO FILL, SET CC AND SET OVERFLOW BIT	& (R(M)) INTO 8		K PUT INSTR BACK INTO B	(R(A)) INTO 8		# MASK BITS 0-5		CHECK FOR SHIFT >= 16			A SHIFT >= 16		# PERFORM LEFT SHIFT		C 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	A CLEAN CHA AZ		1 % FLAG FOR SETTING OV OIT	
REGSTACK - 1 = CPCR FINPUT - 1 = CPCR	MAR2		16 = SAR	A3 L = A3	A3	D = MIRI ASR	FIRE BRZ	ETULUUI - 1 = CPCK	BARK + I = MARZ	BHAK L = BK1			œ		11 = 8	= 111		P ELSE	1 = MPCR	0PC00E - 1 = MPCR					A2 + AMPCR = AMPCR	0P14F - 1 = AMPCR	STEP	EXEC			0P140 - 1 =	FAULT - 1 = MPCR	1 1	0P143 - 1 = MPCR						SRM ~ 1 = CPCR	B = MIR		- 1 = CPCR		6 0	63 = [1]	LII LEO R	16 = [1]	IF FALSE THEN SKIP	- 1 = nrck	NA NA	A 2 L = A 2	2 0 4	1 N N	0 7 E		IF NOT ABT THEN SET LC1	
SINUI																							OP C 0 0 E 1 4 :								0P14F:						0P140																					
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	SET THE CONDITION BILS	03		CHECK FOR 0 IN R(A) 03	N TOTAL COCCUPATION OF THE PARTY AND THE	0 R(A)		E.		NO TYPE ALC LEET CINCLE CHILT	S E S	TIS NO		R	ISOLATE "H" 03		CHECK FOR 0 , "M" FILLO		4				ISOLATE "A" 03	AR2		0 01	SOLATE SHIFT AMOUNT 03	C A A A THIRDHA TOTALS	01 / 1000	080	SHIFT > 16 03		PERFORM REGULACED LEFT SHIFT 03			NEW (R(A)) INTO HIR, 8	C3		ET THE DV BIT ACCORDINGLY		WRITE DUI NEW R(A)	20 20 4 200 4 200 40 40 40 40 40 40 40 40 40 40 40 40 4		FT THE DV BIT	REPARE TO WAITE O INTO R.CA)		03	80	F0	SO TYPE DATE STORE TANK Y	YIE	
-	*	EDUTPUT - 1 = CPCR	1 = MPCR	×	DVBIT - 1 - CPC9 - 4		ETOG - 1 = CPCR	FOUTPUT - 1 = CPCR	UPCODE - 1 = MPCR		t șt	- 64	IFEICH - 1 = CPCR \$	=	A3 AND LIF = 8 K	_	0 E0L B	11	CUNIENISRA - 1 = CPCP X	0		4 = SAR1 15 = LIT	**		= CPCR %	•	LIT AND P = P S	63 = L11	•	IF FALSE THEN SKIP	2 - 1 = MFCR S	= SAR	u t 1	200	L = A2 %	R = HIR, B	NOT A3	E1 101	×	CICCA = 1 = CPCF A	001FUI - 1 = CFCK *	٠	TUCK CCT 104	OVBIT - 1 = CPCR	ge	1 = CPCR	1 - 1	0PC00E - 1 = MPCR	pr s			
				C1408						0P1021																																6142	• 25 10							0P141		
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RXHFIELD - 1 = CPCR COMP = 081 COMP = 082 COMP = 18 = 000 1		A A ADDR INTO E	A LEAF STURAGE UP 7 AUUR		CRCADO INTO B	S (R(A)) BITS C-7 INTO HIR		S (R(H)) INTO B		(R(H)) + 1 INTO HIR, (R(A)) INIO		TO LS BYTE OF	R REFERENCE BR1	K Y ADDR INTO ER2	8 (Y) 1N10 B	SKIP & IF LC2, PUT BYTE INTO LS BYTE							GET 11D	20 - 20			CLEAK LS BYTE OF							K "F" INTO A2				•					×		N RR TYPE CIRCULAR SINGLE EMIFT	SHIFT (R(A)) LEFT CIRCULARLY (R(H))	# BITS 0-5 AND SET CC	A CR(P) INTO B	& (R(H)) INTO HIR					¥ 2
			Tug - 70	A			255 = L11	H - 1 H	0 + 1 × B	B = MIR, BHI	FOUTPUT - 1 = CPCR	B = A3	A S.R.	BMAR = DP.2	EMULIN - 1 = CPCR	IF LC2 THEN STEP ELSE	LS143 - 1 = CPCR	B L = B, CSAR	CONF 24 = SAR	F 4	STATE OF THE STATE	A3 08 B = MIR	FMAR I # ARD	COMP 8 × SAR	EHULOUT - 1 = CPCR	OPCODE - 1 = MPCR		8 = 1 8	œ		OBCORE - LACE	orcode 1 - men		XFC00E - 1 = CFCR		0P15F - 1 = AMPCR	STEP	EXEC	1 1 1 1 1 1	0P151 - 1 =	; ;	- 1						- 1 = CPCR		3737 - 1	1	A2 L = A2	=	= A2, BMI
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			= A31 JUMP	0	0					SET THE CONDITION BITS					CRCH) + 1 INTO RCH)	9 0	Y* INTO BR1	S		D INI (IV) W						ADDR OF BOM) + 1 INTO E(H)			_	-) Y (C-5) PLACES AND SET CC	ISOLATE "M" 0	0	0	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	D		A3 = (R(M))/INSTRUCTION		INTO A2		A2		0		% ISOLATE "A" 0		INTO MAR2	(RCA)) INTO E	0	0		, 0	
			NOT LIT + 1							1 SFI		94	×	€ R1	R CRC		# X							1051 1		C HAR?	A CRC		ĸ				1081 %						8 A 3 ::		S (R(M))		N Y INTO				N ISOL		A ADDR		:	4.3	7 4		
SAVE	A3 GEO LIT	16 = LIT	THEN AS+		LIT - B = SAR	A2 C = 8	1 × 1 × 2 × 2	The state of the s	-	SFICEA - 1 = CPCR	OPCOSE - 1 = MPCR					CONTENISRM - 1 = CPCR	8 L = 9R1	COMP 6 = SAR	AS = d		BHAR = AR2	and a second	BHAR + 1 = HIR	AS AND LIT = B	2 1 1 1 1 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	REGSTACK - 1 = CPCR	OUTPUT - 1 =	OPCODE - 1 = MPCR					LIT AND B = 0	15 = LIT	r Edt U	CONTENTED : 1 - COCO	B 1 = B	COMP 16 = SAR	A3 OR B = A3	IFEICH - 1 = CPCR	A3 R = A2	16 = SAR	A2 + B = A2	A2 AND LIT = HIR	63 = LITF 4 = SAR		A3 AND LIT = 8		1	LINPUL - 1 = CPCK	8 L = A3	A T OR B = 42	ı	0 = A3	
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1 CHECK FOR SHIFT > 16								A SET THE CONDITION BITS				8 RX IYPE STORF AND INDEX FY 1	R (R(A)) INTO Y, (R(H)) + 1 -> R(H)	K ADDR OF Y INTO B				C CR(A)) INTO D		8 Y ADDR INTO FRZ		a other company								% "F" INTO A2											R RR TYPE ALGEBRAIC LEFT DOUBLE SHIFT	SHIFT (R(A), R(A+1)) FFT (R(B)) (0-5)	R JERO FILL AND STI DE SEI DVEDELDE			I ISOLATE THE "A" FIELD	A ADDR OF READ INTO MAR?	(R(A)) INTO B			R TEMP STORAGE OF BEAN		R(A+1)	CRCA+13 INIO B					
AS GEO LIT 1F TRUE THEN A3 + NOT LIT + 1	A3 = B	L11 - B = SAR	A2 C = B	9 = 1 9	I O MAK	HIR B HILL B	_	SELUCY - I H CPCK		*		· ·	•	RXMFIELD - 1 = CPCR X		COMP B = SAR	A 3 × B	ISBA - 1 = CECB			= CPCB	0.0		NIC T A D	במסונתו = ז = רבונא	UPCUDE - 1 = APCK	art.			= CPCR	A2 + AMPCR = AMPCR	0P16F - 1 = AMPCK	STEP	F X E C	•	- 1 =	- 1 "	и	= 1 -	~				B R = B	4 = SAR# 15 = LIT	LIT AND P = P	REGSTACK - 1 = CFCR X	EINPUT - 1 = CPCR S	B I = 42	: SAR1 1 = LIT	BHAR I = BR1 S		LIT OR BNAR = MAR2 &	EINPUT - 1 = CPC9 K	A2 OR B = A2 S	8		REGSTACK - 1 = CPCR	
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	X FOR OVERFLOW TEST			% SET OVERFLOW BIT				NEI ENEM LE DINI				S WRITE DUT SHIFTED (RCA)					X R(A+1)					۲ 2	(R(A) #R(A+1)) INTO Ym y Ym+1	CRCHOO + 2 INTO RCHO	K (R(R)) INTO B					A (KCH)) + 2 INIO KCH)		R TCOLATE *A*			S (R(A)) INTO E		R REFERENCE BRI		K (RCA)) INTO Y*	ADOR OF Y* + 1		S ADOR OF R(A)		R(A+1)	4 (9(A+1)) INTO B		A REFERENCE DR1		% (R(A+1)) INTG Y* +1				PK TYPE ALG LEFT DOUBLE SHIFT		SET CC AND SET OVERFLOW RIT	ISOLATE "H"	
~	A2 R = A3	NOT AS	SET 1C	1 = CPCR		AZ L = AZ, BJ SET LC1	CELLIA = 1 = CFUR	4	B = SAR	A2 R = HIR	16 = SAR	- 1 = CPCR	=	42 4 42 42 44	A2 L = A2		LII OR BHAR = MAR?	EDUTPUT - 1 = CPCR	OPCODE - 1 = MPCR						D - BB4 - 1 = CPCR		LUNK S = SAKJ Z = LII	DAMP 1 - DD2		A	15 1 1 1 1 4 B	AND B = B	1 = CPCR		ISEA - 1 = CPCR	•		2 = BR2	1 = CPCR		8 = \$1			BHAR = MAR2	- 1 = CPCK	HIR			1 = CPCR	OPCODE - 1 = MPCR	~		w	•			15 = LIT
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                                                                                                                                                                                 R SET THE CONDITION BITS
R (R(A+1)) INTO HS WORD OF A2
                                                                                                                                                                                                                                                                 R RX TYPE STORE AND INDEX EY
                                                                                                                                                                                                                                                                                          BF 1
                                                                                                                                                                                                                                                                        R (R(A),R(A+1)) INTO Y, Y+1
                              A3 = CRCH))/INSTRUCTION
"Y" INTO 8
                                                                                                                                $ A2 = (R(A))/(R(A+1)), B
                                                                                                                                            R BITS LOST IN LEFT SHIFT
                                                                                                                                                                                                                                                                                         TEMP STORAGE OF Y INTO
                                                                                                                                                                                                                                                                                                                                                R ADDR OF RCA) INTO KAR2
                                                                                     R(A)
                                                                                                                                                                                                                                                                             8 (R(H)) + 2 INTO R(H)
8 Y INTO 8
                                                                                                                                                                                                                                                                                                                        # (RCH)) + 2 INTO RCH)
                                                                                                                                      SET UP SHIFT AMOUNT
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                                                                                     A TEMP STORAGE OF
            œ
                                                                                                                                                                           S PERFORM SHIFT
                                                                                                                                                                                                                       REFERENCE BR1
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            K (RCH)) INTO
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                                                                        R ISOLATE "A"
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                                                     Y INTO HIR
                                                                                                                                                        F NOT ABT THEN SET LC1
                                                                                                             COMP 16 = SARJ 1 = LIF
            CONTENTSPH - 1 = CPCR
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                                                                                                                                                                          AZ L = A3,BI SET LC1
                                                                              REGSTACK - 1 = CFCR
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A3 OR 8 = A2, BHI
     IF TRUE THEN SKIP
                                   FETCH - 1 = CPCR
                                                                  4 = SAR1 15 = LIT
                                                                                                                                                                                 SEICCA - 1 = CPCR
                                                                                                  EINPUT - 1 = CPCR
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B = MIR
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-B = SAR
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                                                                        A3 AND LIT = B
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                                                16 = SAR
A2 + B = MIR
A3 R = A3
                                                                                                                                                                                                                                                                                                            LII + 8 = MIR
                                                                                                                                                                                              COMP 16 = SAR
                                                                                                                                                                                                                            HAR R = HAR2
                                                                                     BMAR L = BR1
COMP 8 = SAR
                              A3 OR B = A3
                                                                                                                                                                                                                                                                                               COMP 8 = SAR
                                                                                                                                                                                                    12 R = MIR
                                          43 R = A2
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A2 R = A3
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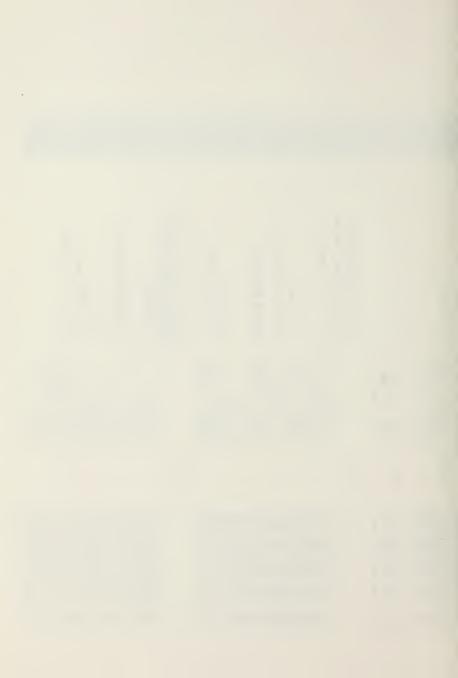
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0.0	IN	Y 0	-		2		BR1		2			15											IRCU	8,0	-2	0					16E			0	(C Y		NIO	2	-		NON	NIO		N 10	TED	PR1					
REFERENCE DO	ADDR OF Y INTO	(RCA)) INTO Y	ADDR OF Y + 1		CRCA+133 INTO		REFERENCE BRI		CKCA+1)) INTO Y+1			0.1											E C.	CRC	0	=					TOR/			(R(A)) INTO	CR		(RCA+1)) INTO B	A3 = (R(A))/(R(A+1)	٠	DESCRIPTION (C-5)	SET THE CONDITION	(R(A+1)) INTO B		CRCA+1) INTO HIR	SHIF	REFERENCE PRI					
101) R 0	(4)) R 0		4		: E R E		Y . 1			Ξ.											TYP	FT	Ê	£					1P S		R(A+1)	ŝ	HAS		A+1	=	9	2 0	H	A+1		A + 1	Ξ	EPE					
9 a d	VDC	C.R.	V DC		4 CB (R REI					% "F" INTO A2											S RR	SHI	3	=					A TEHP STORAGE OF R(A)			×			S CRC			((U)X) AD ADDO K	SFI										
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		CPCR	_		2			9	¥ 4			XFCODE - 1 = CFCR	C R	~				~ .		. ~						= CPCK			-	REGSTACK - 1 = CFCR		COMP 8 = SAR! 1 = LIT	R 2	~			<u>۳</u>			-	- =				CR					C.R	œ
		# CF	AR 1		* CPCR	Š			= CPCK			11	Y H	A MP (HPCR	MPCR	HPCR						-				, "		=	=	CPC		~	CPC				CPC		~		= CF	,	2			- CF	= HPCR
	22	EMULOUT - 1 =	BHAR + 1 L = AR1	8 = SAR								-	A2 + AMPCR = AMPCR	0P17F - 1 = AMPCR				10 (9 (1							 		,	TI AND E B	٦,	L = 8R1	SAR	LIT OR BHAR = HAR2	EINPUT - 1 = CPCR		COMP 16 = SAR	EINPUT - 1 = CPCR	. A3	NUI A2 = A2	AZ + 1 = SAR	SETCCA - 1 = CPCR		16 = SAR	~	DUTPUT - 1 = CPCR	2	BHAK K = HAK2	9		EDUTPUT - 1 = CPCR	
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A S A	BHAR = BR2	HULO	HAR	COMP	A3 = HAR?	B = H1R	3.R	BHAR = DR2	PCODF - 1			XFC	5	0P17F	FXEC			0 P 1 7 C	P 1 7 2	0P173						CONTENISKA	A = A2	A 2 K = B	n =	EGSI	BMAR	OHP	1	EINPUT	B L = A3	OHP	INPU	3 08	•	+ 4	ETCC	A3 L = .B	COMP	B R = HIR	9016	25	¥ '	B = SAK A * R = HIR	. 11	DUTE	0PC00E - 1
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E DI TYPE 4 STADE 25DA. A MITO V.	K (R(H)) INTO B								E RK TYPE CIRCIII AV 1 CET ANIIGI C SUTET	CHARLES CINCOLAN CEFT COURT SHIP!	SMIFT (K(A)#K(A+1)) [LFT CIK, 7 (0-5)	AND SET CC						\$ (R(H)) INTO 8			A T - (D / H) / THE TOUR TION	A A S = CR CHILD INSTRUCTION	D O N I	K (R(M)) INTO A?		K Y INTO A2			K ISOLATE "A"		L TEMP STORAGE OF REAL		0 01111	CREAT INTO E		CREAT INTO PS WORD OF AS			X A3 = (R(A))/(R(A+1))			R PERFORM SHIFT	K SET THE CONDITION BITS			I SHIFTED (R(A+1)) INTO HIF		# REFERENCE BR1								· sc	S RX TYPE STORE ZEGO. C INTO Y	AOOR OF Y INTO D				
	CONTENTSRM - 1 = CFCR		COMP 8 = SAR	0 = HIR	- 1	0PC00E - 1 = MPCK							LIT AND B = B	15 = 1.17	0 101 0	י במר מ	IF INDE THEN SKIP	CONTENTSRH - 1 = CPCR	8 - 18	COMP 16 = SAR	, D = 43		1 = CFCR	K = A2		B = A2	A3 R = A3	4 = SAR1 15 = LIT	8	CFCR	BHAR L = BR1	COMP A = CAP: 1 = 11T	CINDIA - 4 - COCO	III OD DHAD - MADS	CIT OR GILAR - HARZ	P L = A3		2	_			101	L = CPCR	A3 L = A2	COMP 16 = SAR		EDUTPUT - 1 = CPCR		BHAR R = MAR2	B = SAR	A3 R = HIR	16 = SAR	EDUTPUT - 1 = CPCR	0PC 00E - 1 = MPCR				RXMFIELO - 1 = CPCR 1		COMP 8 = SAR	C = MIR	
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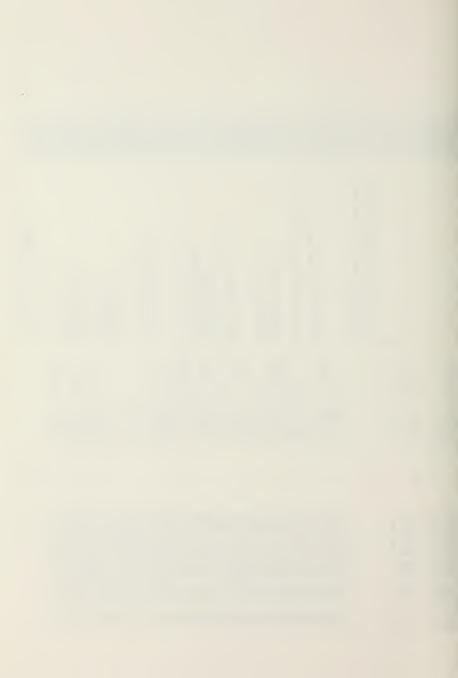
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		% "F" INTO A2										R R TYPE SUBTRACT REGISTER	CRIAD - CRIMO INTO RIAD	CREAN INTO A	S (R(A)) INTO HS WORD OF AC				R (R(H)) INTO E		THE DINI CHANGE TO SELECT	S SET THE CARRY BIT	SET THE OVERFLOW 911			1000		SET THE CONDITION BITS			A COLUMN A C	S (S(A)) - (Ye) INTO R(A).	SET CC. CARRY, AND DV BITS	% (R(H)) INTO B	R Y* INTO PRI			A CR(A)) INTO 8	CREAT INIO ES WORD OF AZ	PEE 984	4 2 2	K (Y*) [HT0 B	K (Yw) INTO MS WORD OF 8		A2 - B = MIR; SET LC2 % (R(A)) - (Y*) INTO HIR					
0PC0DE - 1 = MPCR	* *	~	A2 + AMPUR = AMPUR		FXEC	0.03	0P201 - 1 = HPCR	H				0P200:		CONTENTSBA - 1 = CPCR	9 L = A2; IF LC1 8	COMP 16 = SAR\$ 15 = LIT	A3 AND LIT = B	REGSTACK - 1 = CPCR	~	0 L = 8¢ SET LC2	101 13		œ	INB	B R = B.MIR	I S H SAR	= CPCR	SETCCA - 1 = CPCR X	0PC0DE - 1 = MPCR	* 1			t set	CONTENTSRM - 1 = CPCR		COMP 8 = SAR	0	CUNIENISHA - 1 = CPCR	C 4 D	# 200 F	3 = BR2	= CPCR		COMP 16 = SAR	A2 - B = MIR; SET LC2 &	IF ADV THEN SET LC1	CARRY - 1 = CPCR	CHECKUV - 1 = CPCK	1	0
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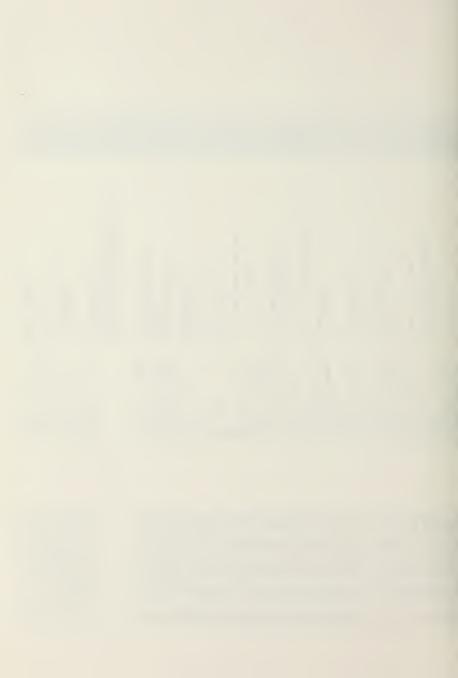
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			SET THE CONDITION BITS			0 / 4 /		## B O INI							AT = (BCH))/INSTRUCTION	-			HIR			0 F		H 13							-	SET THE CONDITION BITS				RCA	SET CC., CARRY AND DV BITS					HIR					HIR							115		
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	2	WRITE OUT NEW RCA)	101			TDAC	A B Y					10 8			N 1 / C		0 A 2		Y INTO MS WORD OF MIR			D MS		- (Y) INTO		CARRY RIT	0 v A I I				WRITE OUT NEW CREATS	1107				J L F A (RY	Y INTO 8				(Y) INTO HS WORD OF		9	9	2	\$ (R(A)) - (Y) INTO HIR							WRITE NEW (R(A)) SET THE CONDITION BITS		
	F R(A)	100	00			CHD	3	108				CRCHOO INTO	:		CHO	SYS INTO B	(R(H)) INTO A2		HS			INI		1		CAS	>				100	00				308	CAF	<u>_</u>			0	ű e		-		-								, F. K.		
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	9	PCR	2	2							4	CONTENTSRH - 1 = CPCR				S S	5				= CPCR			A2 - 8 = HIR; SET LC2	IF ADV THEN SET LC1	~	PCR				PCR	CPCP	MPCR					= CPCR			CR			CONTENICRA - 1 - CECE	;		A2 - 8 = MIR; SET LC2	IF ADV THEN SET LC1	~	PCR			9	ב ב ב	HPCF	
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н	R = MAR2	EDUTPUT - 1 = CPCR									IF TRUE THEN SKIF	SRH	_	COMP 16 = SAR	A3 0R B = A3	IFFICH - 1 = CPCR	A 2	~		A3 = B	CONTENTSRA - 1	B L = A2, BHI	COMP 16 = SAR	H	THEN	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR	'	P R = D, MIR		COULPUL - 1 = CPCR	7	- 1					RXMFIELD - 1	R 2	COMP 8 = SAR	7	<u>~</u> '	COMP 16 = SAR	SPA	1 - 43. DH	COMP 16 = SAR	I H =	THEN	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR		B R = 8, MIR	~ `	SETCCA - 1 = CPCR	-	1
HAU	u :	TP U	V 10	UPCODE				LIT AND B	115 = 111	0 E 01 B	TRUE	TENI	B = 1 B	P 16	20	. E	A3 R = A2	= SAR	B +	8 =	TENI	-	P 16	8 -	A O V	RY	CKOV		=	16 = SAR	TPUT	SETCCA - 1	DPCODE					FIEL	B L = 8R2	80	LIN.	D L = MIR	COMP 16	TENT		P 16	8 -	A 0 A	RY -	CK 0 v		,,	16 = SAR	ETCCA - 1	CPCODE	
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	x "F" INTO A2											~		TABLE OF CLOTON TOUGHT OF TAKE	 \$ (K(A)»K(A+1))-(K(H)»K(H+1)) INIO	S R(A), R(A+1), SET CC, DV, AND CARRY	C ISOLATE "A"					S (R(A)) INTO F	K (R(A)) INTO MS WORD OF A2		R TEMP STORAGE OF ADDO OF CCAN		C D(A14)	O CENT ATTACK	2 - (D(4))/(D(4)4)		A 130CF1E - H-				S (R(M)) INTO BS WORD OF AS		X ADDR OF R(M+1)	K (R(H+1)) INTO R	\$ 0 = (R(M))/(R(M+1))	% PERFORM SUBTRACTION					SET THE CONDITION BITS		S NEW (R(A)) INTO MIR				* REFERENCE BR1	\$ ADDR OF 6(A)			X ADDR OF E(A+1)		S WRITE NEW (R(A+1))				S (R(A),R(A+1))-(YH,YH+1) INTO	
	21: XFC00E - 1 = CPCR	A2 + AMPCR = AMFCR	0P21F - 1 = AMPCR	STEP	EXEC			1			0P213 - 1 = MPCR	•					# B	1 - CAD: 4E - 111	2 4 4 4 4 4	CIII AND U = U	CF	1 = CPCF	B L = A2	COMP 16 = SAR		111 = 111				a		15 = L11 DECETACE 4 = CDCD	2	1 = CPCH		-	2	= CPCR		A2 - 0 = HIRE SET LC2	IF AUV THEN SET LC1	CARRT = 1 = CPCR	CHECKOV - 1 = CPCR		CCA - 1 = CPCR		£=		8 - 1 8	e 8		= MAR2, A3		CPCR	S OR 1 = MAR2		1 - 1 = CPCR	0PC00E - 1 = MPCR				
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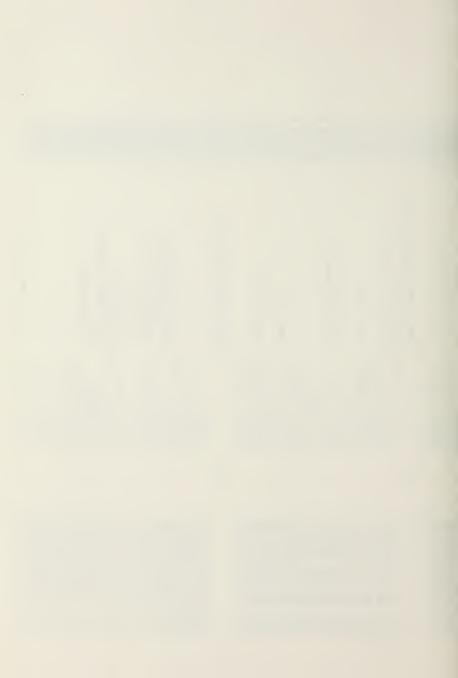
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MKIA) PRIA : 17 SET CC. CARRY AND DV BITS	S ISDIATE *A*		(R(A)) INTO E	CREAD INIU HS WURD OF AZ	SAVE ADDR OF R(A)		R(A+1)	(R(A+1)) INTO B	* * * * * * * * * * * * * * * * * * *		\$ (R(H)) INTO B	& (R(M)) INTO 6		0 0 1 2 1	S ADDR OF Y*+1		R (YH) INTO HS WORD OF A3		N (T+1) NIO	4 PEDEODA CHDIDACTEON			SET THE DV BITS	SET THE COMPLISION DITE	SEL THE COMPLIEN BILLS	NEW (R(A))			NEW (K(A+1))	ADDR OF RCAN		WRITE NEW (RCA))	R(A+1)	CACALLY NEE (RCA-1))	4			RX TYPE EUBTRACT DOUBLE	CET (C. DV AND CARRY RITE	Y ADOR INTO P			R (Y) INTO B	(Y) INTO MS WORD OF AZ		ADDR OF Y+1	(Y+1) INTO B	HIR = (Y)/(Y+1)
	II AND B = F	I = CPCR	1 = CPCR x	COMP 16 = SAR	BHAR L = BR1 S	COMP 8 = SAR; 1 = LIT	2	CPCR #	AT AND LIT = B	.	- 1 = CPCR		B L = BR?	FALLIN 1 4 II COCC		_			trough = 1 = CPCH x	1 551 153		CARRY - 1 = CPCR	CHECKOV - 1 = CPCR &	SETCON - 1 = CPCB &		BR = MIK &	16 = SAR	9 9 9	E # 00 4	R = HAR2		FOUTPUT - 1 = CPCR &	LIT OR BHAR = HAR2 &	- 1 = CPCR		set.		* *	e se				1 = CPCF			COMP 8 = SAR \$ 1 = LIT	ut	A2 OR B = MIR S
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					SAVE ADOR OF READ	:	Z		R(A+1)	RCA	H				SET THE CONDITION BITS		NEW (R(A))			-		WRITE NEW CRCA)	ADDR OF R(A+1)		WRITE NEW (RCA+1))			"F" INTO A2																ADDR OF RCHY INTO MAR2	(R(H)) INTO B		PERCORH ADDITION	ž		
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11	# CC	SA	LIT AND B =	EGSIACK - 1 = CFCR	DHAR L	COMP 8 = SAR	B L = A2	UNP 16 = SARF 1 =	LIT OR BEAR = MAK2 FINPUT - 1 = CPCR	A2 OR E = A2, BHI	- 8	F ADV THEN SET LC1	CARRY - 1 = CPCR	PHI SET (C1	SETCCA - 1		16 = SAR	= -	8	ASR	DAN THE	EDUTPUT	A 3 OR 1	= MIR	OUTPUT	CPCODE - 1 = MPCR		OPCODE 22 1 XFCODE - 1 = CPCH	A2 + AMPCR = AMFCR	0P22F	۵	Ç				0P223				CONTENTSRA	E L = A2	COMP 16 = SAR 1 15	A3 AND LIT = B	REGSTACK - 1 = CPCR	EINPUT - 1	B L = B	A2 + B = MIR	IF ADV THEN SET LC1	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR
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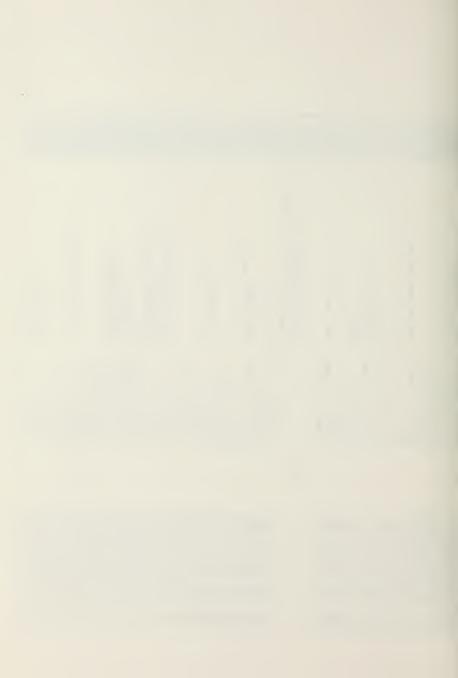
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			R SET THE CONDITION BILS				A LIFE KI LIFE Z ADDJ (K(AJ)+(IF) ->	a contract to the contract of	A CHCAJJ INTO 8	A (R(A)) INTO HS WORD OF A2				K (RCH)) INTO R			0 01 11 1 1 1 1	0 00 0000 00 0101 (12)							4 ADDR OF R(A)			K VRITE NEW (R(A))					R TYPE RK ADD. (READ) +Y -> READ	M SET CC, CARRY AND OV BITS					S (RCH)) INTO B	M (R(M)) INTO PS WORD OF B		% A3 = (R(H))/INSTRUCTION	% "Y" INTO 8	(RCH)) INTO A2		X Y INTO HIR			A (RCA)) INTO HS WORD OF A?		# PERFORM ADDITION								A SEL THE CONDITION BILS
:	BR = MIR, B	~		OPCODE - 1 = MPCR				0000	A - I = CECK	B L = A2	COMP 16 = SAR; 15 = LIT	A3 AND LIT = B	REGSTACK - 1 = CPCR	INPUT - 1 = CPCR		0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	3303		, L	COMP 16 = SAR	A	IF AUV THEN SET LC1	CARRY - 1 = CPCR		A3 R = MAR2, 3MI	16 = SAR	B R = HIR, B	= CPCR		0PC00E - 1 = MPCF					LIT AND B = P	15 = LIT	C E 0 L B	IF TRUE THEN SKIP	CFCR		COMP 16 = SAR		1 = CPCR	2		t = HIR		I = CPCR	R L = A2, BHI			IF ADV THEN SET LC1	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR	IMB	8 R = 8, MIR	16 = SAR	~	SELUCA - 1 = CPCK
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		RX TYPE ADD. CREATINGTY -> REAL	SEI COJ CARRIJ AND OV 0113	3 DINI -		6		CITIMIN OF WORLD OF MIR			INIO G			PERFUAR ADDITION							SET THE CONDITION BITS					"F" INTO A2				9						TYPE RR ADD DOUBLE, (R(A)). B(A+1)) +	(RCH), RCH+1)) INTO RCA), RCA+1)	SET CC, CARRY AND OV BITE				(RCH)) INTO E	(R(H)) INTO HS WORD OF AZ		A00R OF ECH+1)	(R(H+1)) INIO B	MIR = (R(H))/(R(h+1))			# ISOLATE "A"		M LEMP STORAGE	(R(A)) INTO E			
0PC00E - 1 = MPCR				= L = CT CR	6 L = UR2	COURT B = SAR	נוני		X 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	0000 - + - + 031	י ני	110 CV = T 3	2	AZ + B II II K	IF ADV THEN SET LC1		CHECKOV - 1 = CPCR		B R = HIR, B				0PCODE - 1 = MPCR	~	p¢.	= CFCK X	A2 + AMPCR = AMPCR	OP23F - 1 = AMPCR	L (1)	-			1 11	•	r set	· we	54		LIT AND B = P S		1 = CPCR	UT - 1 = CPCR	E L = A2	=	2	CPCR	A2 OR B = MIR K	A S R = B	4 = SAR1 15 = LIT		- CF CF	١	- 1 = CPCR -		= SAR 1 1 = LI	
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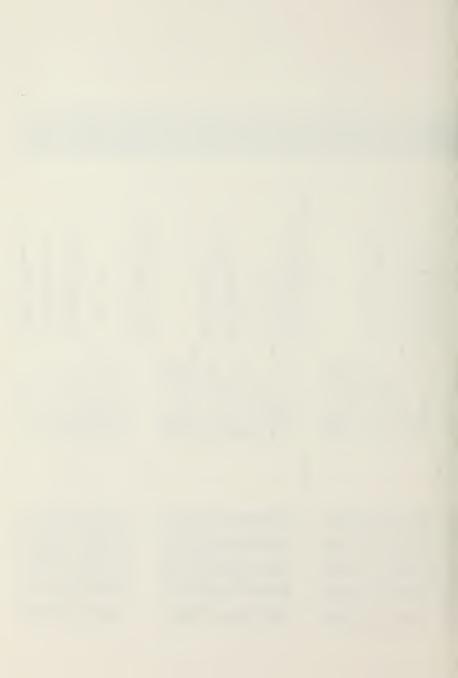
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X HEA-22		x A2 = (R(A))/(R(A+1))					K SET THE CONDITION BITS							* REF 6R1	K R(A)		* VRITE NEW RCAD				# RI TYPE 2 AND DOUBLE	9	A REALFREATILE SEL CLE CARLE AND UV BILS	\$ Y* 1FT0 ER2		% (Y*) INTO 8	K (Y*) INTO MS WORD OF A2				A HID = CYELLON					A TEMP STOPAGE FOR R(A)	\$ (B(A)) INTO F	K (R(A)) INTO HS WORD OF A2		N R(A+1)		x = Az = (R(A))/(R(A+1))	A PERFERN ADDITION				X SET THE CONDITION BITS				A NEW (K(A+1))	S WRITE NEW (RCA+1))	
	FINFOL - 1 = CPCR	42 4 B = 429 BRI	THE PART OF LA	CARDY = 1 = CPCP	CHECKOV - 1 = CPCR	BM13 SET LC1	SETCCA - 1 = CPCR	BHI	B L = A2	COMP 16 = SAR	A2 R = HIR		FOUTPUT - 1 = CPCR	ASK	PHAR K = HAKZ	2 C Z		0PC00E - 1 = MPCR			0P231:		OSGS - F - MGSINGINGS	4	COMP 8 = SAR	FAULIN - 1 = CPCR	8 L = A2	COMP 16 = SAR	+ 0	CORP 8 = SAR	A2 08 B = KIR	A3 R = A3	4 = SAR; 15 = LIT		REGSTACK - 1 = CFCR	6-14R L = 8K1	EINPUT - 1 = CPCK	B. L = A2	COMP 16 = SAR; 1 = LIT	LIT OR BHAR = HARZ	CINPUT - 1 = CPCP	AZ ON B = AZ, BHI	THE POST AND A PERSON OF A PERSON AND A PERS	CAROY - 4 - COCO	CHECKOV - 1 = CPCR	BMI SET LC1	SETCCA - 1 = CPCR	IHB	B L = A2	COMP 16 = SAR	N	COUTPUT - 1 = CPCR	
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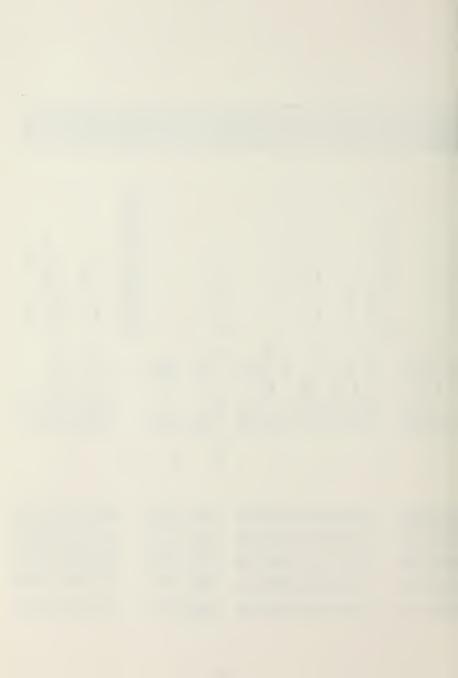
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RREF BR1			and it men than)	*			(1,1,1,1)		A AUDR OF Y INTO 6				X (Y) INTO MS WORD OF A2				X (Y+1) INTO B	8 HIR = (Y)/(Y+1)					X TEMP STORAGE OF R(A)	0 0111 (1470)	A CRUADA BATTO BE SEED OF AN	A CACAL INTO ES MENO OF AC	R R(A+1)			R FERFORM THE ADDITION					SET THE CONDITION BITS				8 (R(A+1))	8 WRITE NEW (RCA+1))	K REF PR1			* (R(A))					% "F" INTO A2					
ASA PHAR R = HAR?	CZ C	MITPHI - 4 - CPCO	. t = HPrp			0P233:			- 1 = CPCR	B L = 6R2	COMP 8 = SAR	EMULIN - 1 = CPCR		COMP 16 = SAR	PHAR + 1 L = BR2	COMP 8 = SAR	EMULIN - 1 = CPCR	= MIR	A3 R = B	4 = SARI 15 = LIT	LIT AND B = R	= CPCR		CONF B = SAR		SAR 11 = 1.17					IF ADV THEN SET LC1	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR		CCA - 1 = CPCR	B#1	COMP 44 - 540		118	1 = CPCR		PHAR R = MAR2	= SAR			OPCODE - 1 = MPCR			0PC00E24: XFC00E - 1 = CPCR	AZ + ANFOR = ANFOR	OF24F - 1 = AMPCK		,	0P24F: 0P240 - 1 = HPCR
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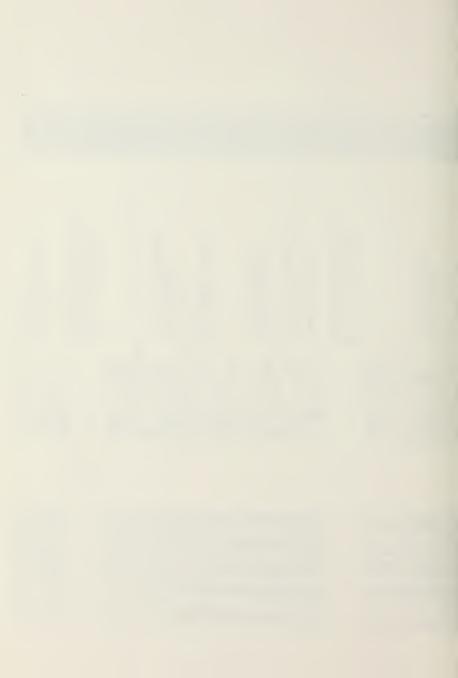
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			% IYPE RR COMPARE, (RCA));(RCH))	A SET CC. CARPY AND DV BITE	X (R(H)) INTO B	X TEMP STORAGE OF (R(H))		S (R(A)) INTO B			(RCH)) INTO HS WORD OF B. MIR	STATE CONSTRUCTOR OF TO	SEL INE CONDITION BILS								_	8 RI TYPE 2 COMPARE, (RCA)):(Y*)	A SET CC. CARRY AND DV BITE	= CPCR % (R(A)) INTO B	# IEHF STORAGE OF (R(A))	= CPCR % (R(M)) INTO B			E (S(A)) INTO A2		0 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	CAN INTO HE LIBE OF D		S SET THE CONDITION BITS	, ~								TYPE RK COMPARE, (RCA)):Y	K SET CC. CARRY AND DV BITS					S CR(H) INTO B			A3 = (RCE))/INSTRUCTION	*Y* 1N10 B	R (R(H)) INTO A2		N Y INTO MS WORD OF MIR		S (R(A)) INTO B	R (RCA)) INTO KS WORD OF A?	
0P241 - 1 = MPCR 0P242 - 1 = MPCR	-			-	SRM - 1 = CPCR	6 = MIR	A 3 = B	CONTENTSRA - 1 = CFCR	-	COMP 16 = SAR		0.00	1 = 0108	100	AZ - B = MINT SET LCZ	IF ADV THEN SET LC1	CARRT - 1 = CPCR	CHECKOV - 1 = CPCR	0PC00E - 1 = MPCR		_			SRA - 1 = CPCR		= CPCR	C L = 8R2, BHI	COMP 8 = SAR		SAR	0000		~	CR		- B = MIRs SFT 1.C2	IF ADV THEN SET 1C1	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR	OPCODE - 1 = MPCR		· sc			IIT AND B = B	15 = LII	0 601 8	IF TRUE THEN SKIP	CPCR		COMP 16 = SAR		CPCK				A3 = B	= CPCR		
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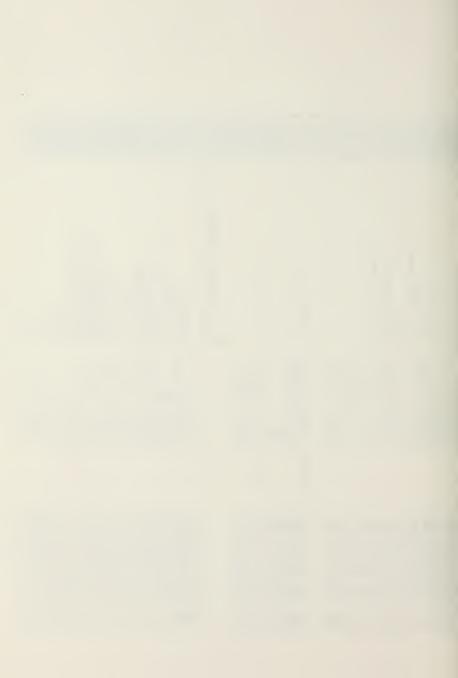
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S ET THE CONDITION BITS							2		A SEL CENTRAL MAD OF BILD				a o ini co				S (R(A)) INTO 8										***	: 544	% "F" INTO A2					*					TYPE BE CAMPARE DOUBLE DEGICAL	% (R(A), R(A+1)) ; (R(H), R(K+1)),	K SET CARRY, CC, AND OV RITS			% ISOLATE "A" FIELD		K (R(A)) INTO A				R(A+1) INTO B	x A2 = (R(A))/(R(A+1))	TOUR TENEDO		
COMP 16 = SAR 0 = MIR SETCC - 1 = CPCR	виі	A2 - B = MIR# SET LC2	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR	0PC0DE - 1 = MPCR		10000		00000		240 - 240	COLUMN COLUMN	1 = 1 = LLCF	AL H MIK	COUP IS MAK		CONTENISKA - 1 = CPCR	1	CONFIDENCE	GOGO COLON		110	77 - 0 = ulul 35 LCZ	CARRY A CRCR	CHECKAN CPUR	OPCODE - 1 = MPCR			OPC00625: XFC006 - 1 = CPCR	A2 + AMPCR = AMPCR	0P25F - 1 = AMPCR	STEP	FXEC				OBSES - LABOR	-	00000				SAR		CR	1 = CPCR	B L = A2	COMP 16 = SARJ1 = LIT		CPCK	A2 OR B = A2	- E		
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(RCH) INTO 8			K ADDR OF REMAIL	(RCM+1)) INTO B	B = (R(H))/(K(H+1))										A RI TYPE 2 COMPARE DOUBLE	(R(A) ,R(A+1)):(Y+,Y++1)	SET CC. CARRY, AND OV DIIS			ISOLATE "A" FIELD			(R(A)) INTO HS WORD OF AZ		R(A+1)	(R(A+1)) INTO B	A2 = (R(A))/(RA+1))	ISOLATE "N" FIELD				0 0 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	S (**) INIO HS KORD OF AN		% ADDR OF Y* + 1		X (Y*+1) INTO B	$B = (\gamma *)/(\gamma * + 1)$	SET THE CONDITION BITS								1040000 L 00000 X0 L0X1	X IITE NA COUGLE CONTANE XCR(A).R(A+1)):(Y.Y+1)	CET CC. CARRY AND DV BITS	T SEL CEN CARRI AND UT BILD			S (Y) INTO B	R (Y) INTO MS HORD OF A2		ADDR OF Y+1
REGSTACK - 1 = CPCR FINPUT - 1 = CPCR x	P (= A3	COMP 16 = SARJ 1 = LIT		•	~	SEICC - 1 = CPCR	FH1	A2 - B = MIRJ SET LC2	1F ADV THEN SET LC1	CARRY - 1 = LPCR	CHECKOV - 1 = CPCR	OPCODE - 1 = MPCK	ut	•	*	set.	•	E H H E	-1	w?	C.R.	1 = CPCR x	ut.	- 111	~	CP CR	b t	8 = 1	15 = LIT	REGSIACE - I = CPCR	BARK L = BK2	2000	B = A3	-	LIT OR BHAR L = KAR2 %	COMP 8 = SAR	est cr	A3 OR B = B, MIR & B	ut.	E H I	A2 - B = MIRJ SET LC2	IF ADV THEN SET LC1	(AKK) = 1 = UPUK	CHECKOV = 1 = CPCH	01 CODE - 1 - 11 CN	P sel				RXMETELD - 1 = CPCR *		COMP 8 = SAR		B L = A2 %	=	
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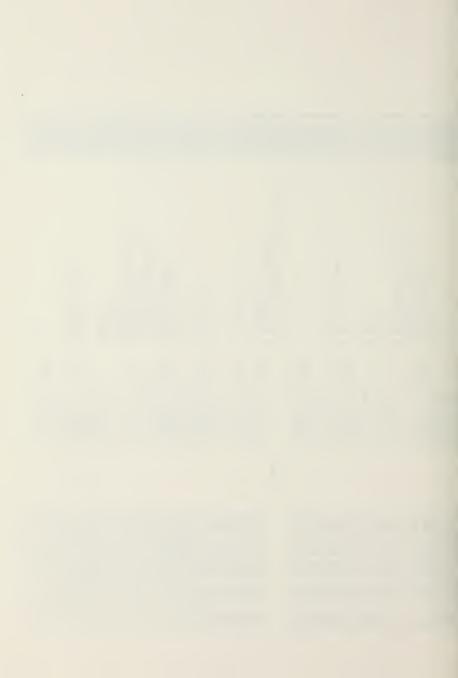
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							WORD				A+1)	0 K B																					Y CR	= (v						101		9 NC							
	9	Y+1)				۵	(RCA)) INTO PS WORD OF			(R(A+1)) INTO B	/ CRC	SET THE CONDITION BIIS																					I I PL	CRCH							R(A+1)	4 6	2			604		HILLY COCASIAN X COCHA		CONDITION BITS							
	NIO	HIR = (Y)/(Y+1)		1	.	1 10 10	INTO			- I	3	CON									"F" INTO A2												MUL	×			. Y		* TEMP STORAGE			ACATI ITIO DAR	-	1	=	PENN INTE HARD	CRCM) INTO F		PRODUCT IN AS	CON							
	1 (1				ISULATE	6	6			4:0	= (R	THE																					TYPE	A+1)			LATE		S	-	2 :		1	TODIATE SHE		2	:		TOAC	SET THE	3		£R1	_		-	2
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	æ	wt		•	*	~	**	111	w	*	₩	wt		23					•	e 1	×					•					æ	ut	set.	sK.			wit		**	٠	٠.		•		t	-		t ø	t ac	×	*		*	set.		٠	*
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8 × SAR	TULIN - 1 = CPCR	AZ OR B = MIR	51	4 = SAR1 15 = LIT	AS AND LIFE	FINE T - 1 = CPCR		- S	LIT OR BHAR = MAK2	- 1 = CPCR	A2 OR B = A2, DH1	SEICC - 1 = CPCR		Ī	IF AUV THEN SET LC1	CARRY - 1 = CPCR	THECKUY - 1 = CPCR	OPCODE - 1 = MPCK			AFCODE - 1 = CPCR	AZ + ANPUR = ANPUR	-							=						= SAR1 15	LIT AND B = P	REGSTACK - 1	914	SAR		-	•					4 11						BHAR R = HAR2	•		
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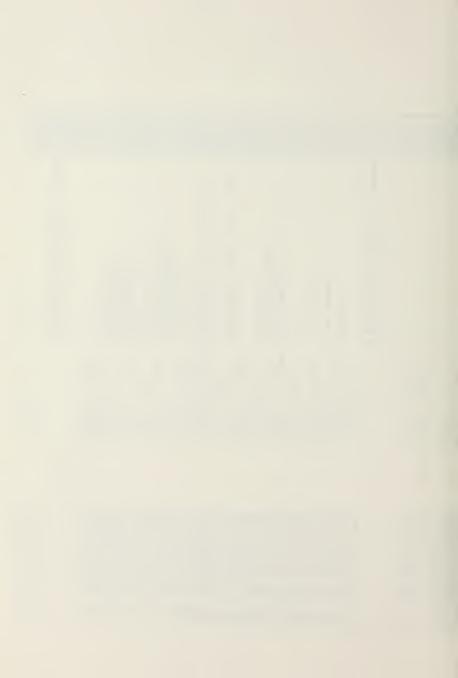
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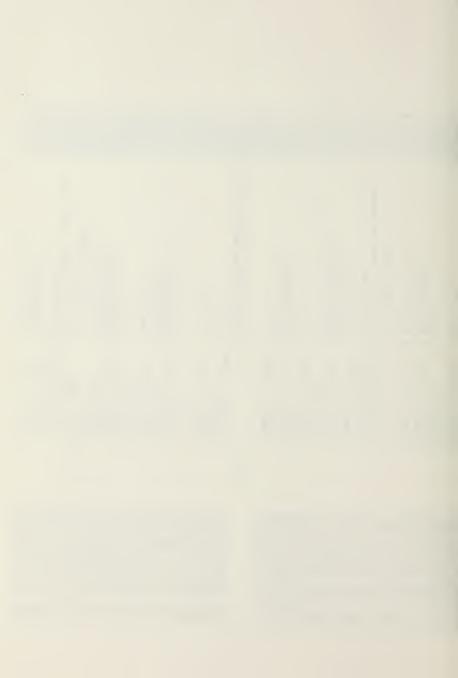
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8 °F° INTO A?	S TYPE RR DIVICE (REGISTER) S RALA, SKA MALA, SKEMAINDIR	# ISOLATE "A" # ISOLATE "A" # TEMF STORAGE # (R(A)) INTO B # R(A+1) INTO P # R(A+1) INTO P # R(A+1) INTO P		X CERA IN 0 B 1 X CERA X	X PI TYPE 2 DIVIDE (INDIRECT) X (R(A),R(A+1))/(Y*) = R(A+1), REHAINDER X INTO R(A), SET CC AND OV X ISOLATE "A"
OPCODE27: XFCODE - 1 = CPCR A2 + AMPCR = AMPCR OP27F - 1 = AMPCR STEP	0P27F: 0P270 - 1 = HPCR 0P271 - 1 = HPCR 0P273 - 1 = HPCR 0P273 - 1 = HPCR	4 = S.A.1 5 = L.11 L(1 AND D = U RCGSICK - 1 = CPCR RMR L = BR1 COPP B = S.A.R COPP B = S.A.R COPP COPP B = S.A.R COPP B = S.A	A 2 0 R D = A 2 A 3 AND LII = 0 15 = LIT = 0 16 E SIT C C C R C NP 16 = SAR C NP 16 = SAR D N - 1 = CPCR IF LC 1 WR SET LC 1 E LC 1 WR SET LC 1	A3 = 0 A5 = MIR SEICA - 1 = CPCR SEICA - 1 = CPCR SEICA - 1 = CPCR MAR R = MAR2 E001P1 - 1 = CPCR A3 = MIR C001P11 - 1 = CPCR A3 = MIR C001P11 - 1 = CPCR	0P271:
5 6 9 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	18A0 0000 0000 0040 1800 0000 0000 1800 0000 0000 1800 0000 00	4 8 6 9 9 6 4 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9	4809 CCS CONO COFFO 4809 CCS CONO COFFO 251C COOD CODE COFFO 251C CODE CODE COFFO 251C CODE CODE COPFO 251C CODE COPFO 251C CODE CODE COPFO 251C CODE CODE COPFO 251C COPFO 251C CODE COPFO 251C	2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	4809 OC40 883C COFO 80FC OD60 COBO 0080 4809 2C55 0830 COFC
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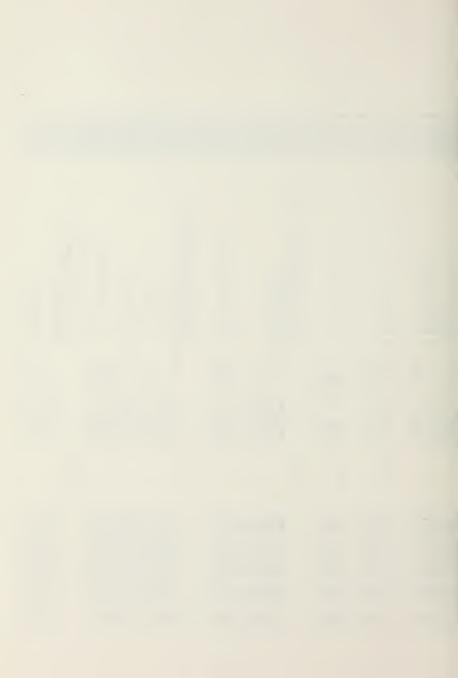
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R TEMP STORAGE	K CRCADO INTO B		X R(A+1)			3 AZ =(R(A))/(R(A+1))	A ISULAIE "H"		X Y* INTO E		S (Y*) INTO B			K (R(A),R(A+1))/(Y*)	STEP ELSE SKIP & CHECK FOR OVEPFLOW		A CLEAR THE DV BIT			# SET THE CONDITION BITS	A REF BRI				X R(A+1)					A TYPE RK DIVIDE (CONSTANT)	A CREADING AND DESCRIPTION OF THE RESIDENCE RESIDENCE RESIDENCE OF THE PROPERTY OF THE PROPERT	ISOLATE "H"		A CHECK FOR F = C	T (R(K)) INTO B			A A3 = (R(F))/INSTRUCTION		K (R(H)) INTO A2	A PO CROW SH OTHER F	CLEAR HUW OF AN		R A3 = Y/INSTRUCTION		***************************************	
REGSTACK - 1 = CPCR BHAR L = BR1 COMP B = CAD	· ·	B L = A2	COMP 16 = SAR BMAR + 1 = 8	REGSTACK - 1 = CPCR	EINPUT - 1 = CPCR	2	15 = LIT	-	EINPUT - 1 = CPCR	B L = BR2	FAULTN - 1 = CPCR	B L = B1 SET LC1	COMP 16 = SAR		SFIOVALL 4 - CPCP	IF LC1 THEN SKIP	CLEAROV - 1 = CPCR	I.R.	3 = 0	SETCCA - 1 = CPCK	ANK BAKB B - HABS		EDUTPUT - 1 = CPCR	A3 = MIR	BMAR + 1 = B	EDUTPUT - 1 = CPCR	OPCODE - 1 = MPCR			012/21		A3 AND LIT = B	15 = LIT	TO TOUG THEN SAID	3 LI CPCR		COMP 16 = SAR	A3 OR B = A3	1FE1CH - 1 = CPCK	A3 R = A2	+		A3 R = A3	A3 OR B = A3	A3 R = B $4 = 54Rs$ $45 = 4.11$	III AND R = R	
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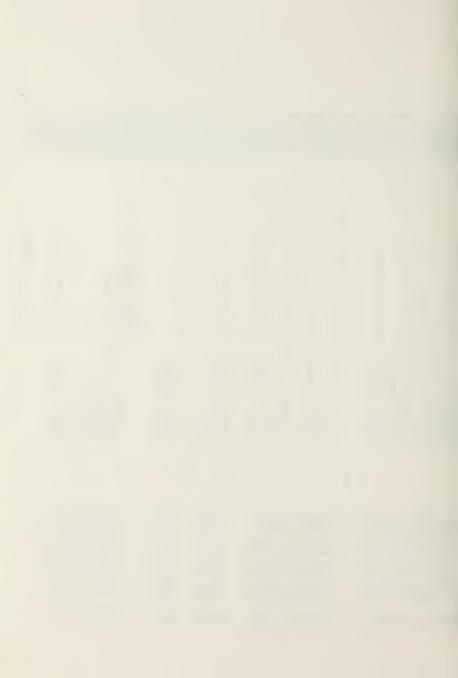
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CC	EINPUT = 5 AR EUR BY ET	EINPUT = 5.84 0.01	COURT COUR
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REMAINDER INTO HIR R(A)	OUDTIENT INTO RCA+1)	R(A+1)	R(A+1) INTO HARE	OUDTIENT INTO MIP					FF INTO A2												A TIPE KM AND (NEGLOTEK)	C (R(A)) INTO R	USED AS TEMP	R (R(H)) INTO B	•		R(A)			SET THE CONCILION BILS			S DI TYDE 2 AND CINDIDECT.	COCAN AND CYM) = RCAN, SET CC	C CLU E			% (Y*) INTO B			* (R(A)) INIU B			E SET THE CONDITION BITS				TYPE RK AND (CONSTANT)		ISOLATE "H"		% CHECK FOR M = 0		K CK(E)) INIO B
A2 = HIRJ ASR 8 BHAR R = HARZ 8	COUTPUT - 1 = CFCR \$		- 1 = CPCR		FOUTPUT - 1 = CPCR	0PC00E - 1 = MPCR	~		XFCODE - 1 = CPCR		0P30F - 1 = AMPCR	STEP	EXEC	~	0P300 - 1	- 1	1	11	* 1			CONTENTED A CONTENT	5	SRM - 1 = CPCR		MIR, P	A3 R = HAR2 8	16 = SAR	I = CPCR			* 1			ADAD = + - MADINATION	10 10 11	COMP 8 = SAR	CPCR	B = MIR		- 1 = CPCH	E = A2,8HI	AZ AKO B = MIKA B		A TOTAL I I COUNTY	96				LIT AND B = B S				CONTENTSEM - 1 = CFCR
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			8 "Y" INTO 8			א ו ואום חוא		A CRIAD INIO B			2010 100111011000 01100					RX TYPE AND	\$ (R(A)) AND (Y) = R(A), SET CC				N (1) INIO B		O OLNI (CA) O)				SET THE CONDITION BITS				% "F" INTO A2									R RY TYPE OR (REGISTER)	A CREAT OR CREATE = REALL SEL CC	A CHIALL INIU B	S CREED INTO B			I R(A)			A SET THE CONDITION BITS			A RI TYPE 2 OR (INDIRECT)	T (R(A)) OR (YN) = R(A), SET CC
80 e J	COMP 16 = SAR	A3 OR B = A3	TCH - 1 = CPCR	A3 R = A2	1 S H S H S		COSC 1 4 4 CONTRACTOR	-	A2 AND B = HIP. F.	CONTENT - 4 - CRCB		11 2 11 2	UPCODE - 1 = MPCh			0P3C31		- 1 = CPCR	B L ≈ BR2	4	D - WIR	2 2 2 2 4	and - t - Adol		A2 AND 9 = H19. B	8 00 1 - 1 = CDCB		PC00E - 1 = MPCR			0PC00E31: XFC00F - 1 = CFCR ;	A2 + AMPCR = AMPCR	OP31F - 1 = AMPCR	7 1 2 1	1 = NPCR	0P311 - 1 =	1	11 11		0P310:	000	-	CONTENTSRM - 1 = CPCR		A 2 08 8 = M18 B	A3 R = MAR2	16 = SAR	TFUT - 1	- 1 = CPCR	0PC00E - 1 = MFCR		0P311:	•
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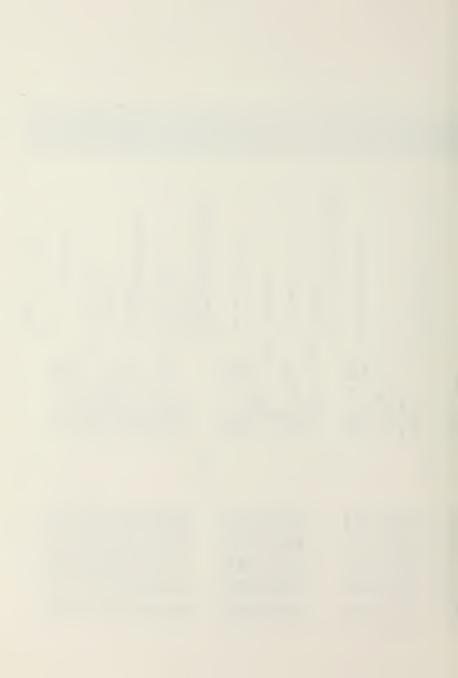


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                                                                                        R PK TYPE OR (CONSTANT)
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                                                              SET THE CONDITION BITS
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                                                              SETCCA - 1 = CPCR
OPCODE - 1 = MPCR
           COMP 8 = SAR
EMULIN - 1 = CPCR
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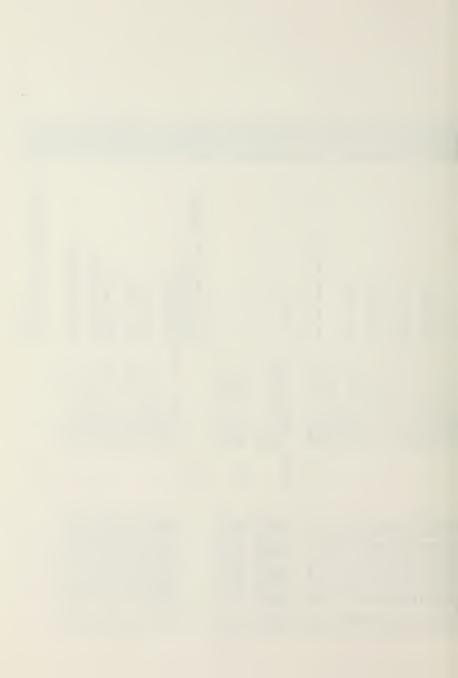
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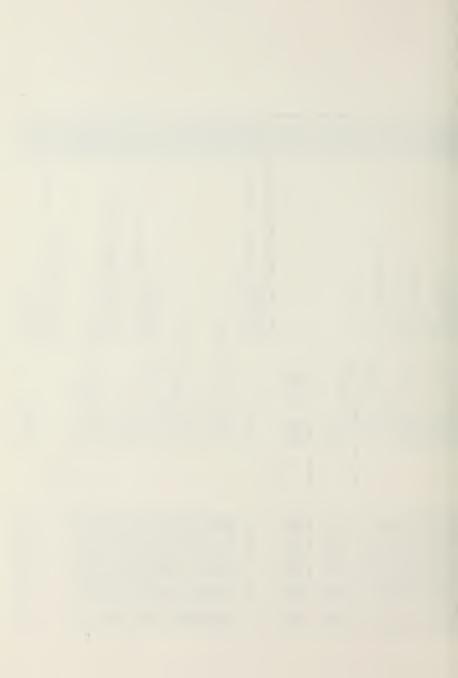
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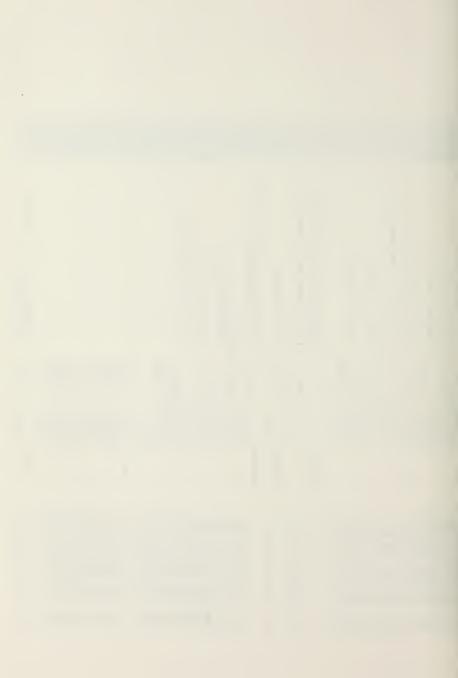
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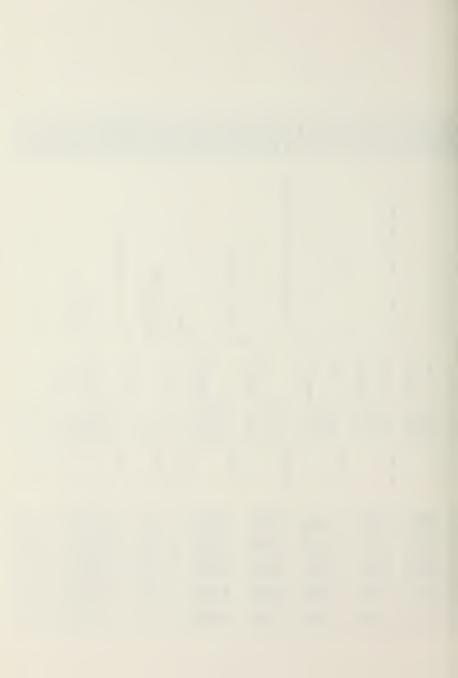
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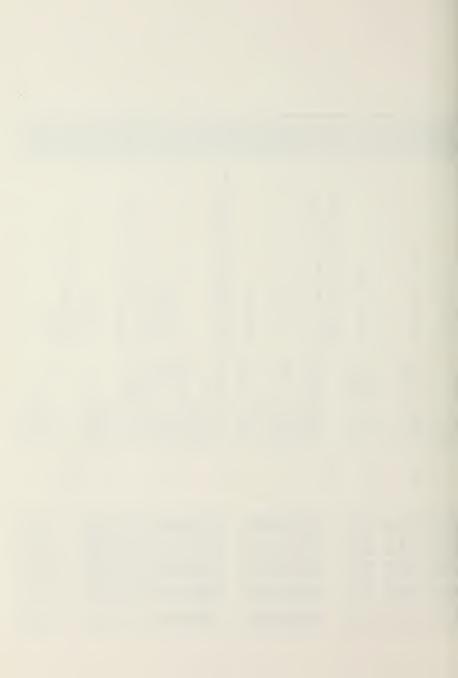
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A SET THE CONDITION BITS		# SET BIT 14 OF (Y)	000 01101 A 0001010 9	NEGLONE - INC		R PUT CC DIT 9 INTO LS BIT		R SET BIT 9 TO OF AND PESTURE A1			4 SET (Y) E17 14,15		A RESTORE Y INTO BR2			× 1		A NOT ASSIONID. GENERALES INTERRUPT	S JUMP TO FAULT HANDLING ROUTINE			X NOT IMPLEMENTED		% THIS ROUTING ANALYZES THE UP OPCODE	IELP RETURNED IN A2		ELSE SKIP	CASI	R ISOLATE THE :A: FIELD		X B AND A2 = :A: FIELD		A LEST FOR NOT ASSIGNED INST.						w											•	4	X CC RETURNED IN B	
	SAR		I O I I SAR	ENULOUI - 1 = CPCR	0PC00E - 1 = MPCR	P353: A1 C = A1,CSAR	25 = SAR	A1 AND 8110 C = A1	9 ≈ 3 8	30 = SAR	LIT OR O C = MIR	3 = LIT1 18 = SAR	A 3 = BR2	- 1	0PC00E - 1 = MPCK		1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	or college i	FAULT - 1 = MPCR	-		,	-	0PC00E40:	XFCODE - 1 = CPCR	A2 FOL 1	٠	0P401 - 1 = MPCR	R = B		W O D	LII GEO R	12 = 111	EALL I - 4 - EDSE	AZ + AMPCR = AMPCR	JUMP40 - 1 = AMPCR		EXEC			11 -	DPUDXOX - 1 = MPCR		1	<u>"</u>	NJTIMP - 1 = MPCR	- 1 -		- 1	0P40X13 - 1 = MPCR	000000000000000000000000000000000000000	CHECKCC - 1 = CPCR	
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THEN SET	= CPCR N SEI		E CPCF THEN SET T = RPCR	THEN S	R = A2 = SAR HOT LST THEN SET LC1 OX - 1 = MPCR s	HPCR	R = A2 = SAR NOT LET THEN SET	HPCR	
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. B	0 0 0 0 0 0 0		00 E	= A2 SAR T LS	= A2 SAR IT LS	1 1	= A2 SAR		= A2 SAR
O EOL B IF FALSE OP40X - 1	CHECKCC D GIR O IF FALSE OP40X -	CHECKCC	CHECKCC - 1 = CP LII EOL E 3 = LII 1F FALSE THEN SE 0P40X - 1 = hPCR	A1 R = A2 77 = SAR A2 1F NOT LST THEN SET LC1 0P4 0x - 1 = PPCR	A1 R 229 = 5	0P40X 9A11 S1EP 0P43X	A 1 R A 2 A 2 B A 2 B A 2 B A 2 B A 2 B A 2 B A 3 B A	OP4OX VAIT STEP OP4OX	A1 R 30 =
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C1 LLSE SKIP		R MACHINE STOPS				# DECOLE THE SFS FIFLD					•			A DECODING PROFLEM			~	K THIS ROUTING LOADS (RCM)) INTO P.	S IYPE 9R	SKIP # ABORT JUMP, GET NEXT INST.		S B = 1M1 FIELD			(B = (R(H))	2				(K(R)) -> P			# H	SKIP & ABURI JUMP, GET NEXT INST.								% A3 = (R(M))			SKIP % ABORT JUMP, GET NEXT INST.		% (R(H)) + 1Y1 = Y				% Y INTO PAR		~	A THIS ROUTINE LOADS Y INTO P.	R IYPE RX.	>= ± ± ± ± ± ± ± ± ± ± ± ± ± ± ± ± ± ± ±	•		(k) = (k)	
IF LST THEN SKIP	OP40X - 1 = HPCR	WAIT	SIEP	DP40x - 1 = HPCR		XFC 00F - 1 = CPCR	AZ + AMPCR = AMPCR	DP40F - 1 = AMPCR	STEP	EXEC					Drace - 1 = HPCK	-				IF LC1 THEN STEP FLSE	OPCODE - 1 = MPCR	A3 AND LIT = B	15 = LIT	REGSTACK - 1 = CFCR	11	A1 B = A1	1		A1 L = A1	Aluk B = Al	10		- 1	ALL LLI INEN SIEP ELSE	BURF - 1 = FFCK	-	15 = [1]		F TRUE THEN		FINPUT - 1 = CPCR	B = A3	IFETCH - 1 = CPCR	IF LC2 THEN SKIP	IF LC1 THEN STEP ELSE	BUMP - 1 = MPCR	A3 + B = B	A1 R = A1	16 = SAR	_	A1 0R B = A1	0PC00E - 1 = MPCK				RXMFIELD - 1 = CFCR	e L = BR2	= SAR	# CHOLIN - 1 = CPCR	74 - 4 74
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				RCAD			R(A),
8 (Y) INTO PAR	X	X INDEX JUNP X "F" CODE RETURNED IN A?	W W W	TO TYPE INDEX JUHP TO THE (R.CA.) HE DAY AND (R.CH.) IN B RETURN (R.CA.) IN B SKIP	X DECREHENT (R(A)) X BETTIE NET RRAND VALUE IN R(A) X B CONTAINS (R(H)) X CLEAR THE OLD PAR X CREATE NEW PAR	* RI TYPE 1, LOCAL JUHF INTIRECT * IF (CC) ME C, ((P) + D) INTO P * FUT (CC) INTO LS 2 DITS CF 8 SKIP * (P) + D = P	TYPE INDEX JUHP (K(A)) NE 0, (R(A)) - 1 INTO NIO P T (R(A)) IN 6
16 = SAR A1 L = A1 A1 OR D = A1 OPCODE = 1 = HPCR	RII - 1 = MPCR	11:	0P410 - 1 = HPCR 0P411 - 1 = HPCR 0P412 - 1 = FPCR 0P413 - 1 = HPCR	CONTENTSRA - 1 = CFCR 0 EOL 0 THEN STEF ELSE 0 PCODE - 1 = HPCR	A2 - 1 = H1R E OUTPUT - 1 = CPCR CONTENTSM - 1 = CPCR AR = A1 16 = SA A1 L = A1 A1 OR D = A1 OPCODE - 1 = HPCK	# RI CHECKCC - 1 = CPCR	S PK S I F CONTENISRA - 1 = CFCR S PU D E GOT I F TRUE THEN STEF ELSE SKIP OPCODE - 1 = MPCR
}	0P401 s	0 P C 0 0 E 41 :	0P41F:	301430		0P411:	064121
0020 60F0 00F0 00H0	0 0 4 C	0060 0000 0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	C 0 6 0 0 0 F 0 0 0 4 0 0 0 F 0	COF 0 006 0 006 C COF 0 COF 0 00F 0	0900 0400 0400 0400	0000
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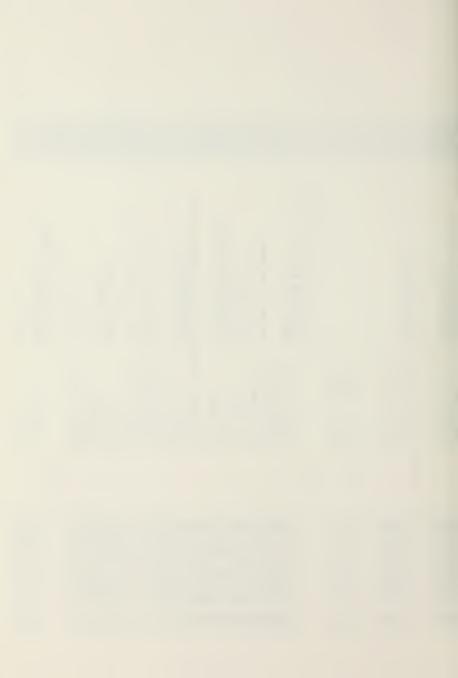
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DECREMENT COLAND	AUDRESS OF READ INTO MARE		K (R(A)) - 1 INTO R(A)	R "H" FIELD IN A3			C RETURN COCHA IN D		UT Y IN B	1N10 B							RX TYPE INDEX JURP	IF (E(A)) NE 0, (R(A)) - 1 = (R(A)),	CY INTO P	MINIO OF A THE	X ISOLATE "A"	R(A) INTO MAR?	CR(A)) INTO B		_	A ADVANCE THE FAR BY 1 AND CALL OPCODE	DECREMENT CREAM	JIPUT NEW VALUE OF RCA) IN RCA)	RESTORE INSTRUCTION IN B	ANALYZE THE "H" FIELD	ADDRESS OF Y IN BR2			EAR OLD PAR		CREATE NEW PAR			RR TYPE JUMP, LINK REGISTERS	"F" INTO A2											JUMP. LINK RESISTER
	×		×			2	-	S	F P.	≻						.	₩ ₩		S ;		×	R R	2		×.	×				N A						X CF			R R	× = =				34							D
A2 - 1 = M1R	10	16 = SAR	ы	A3 AND LIT = A3	15 = L11	IF TRUE THEN O = OF SKIP	I = CPCB		IFEICH - 1 = CPCR	B + 6	COMP 44 = CAD	10 + 0 T T T T T T T T T T T T T T T T T	A1 L = A1	0PC00E - 1 = MPCK	4				0	4 = SAR 15 = 11		REGSTACK - 1 = CFCR	FINPUT - 1 = CPCR	8 EOL C	IF TRUE THEN STEP ELSE SKIP	BUMP - 1 = MPCR	A2 - 1 = M18	EDUTPUT - 1 = CPCR	A3 = B	RXHFIELD - 1 = CPCR	8 L = 8R2	CONP 8 = SAR	A1 B = A4	COMP 16 = SAR	A1 L = A1	A1 0R B = A1	UPCODE - 1 = MPCR		F 42:	XFC00E - 1 = CPCR	4 ×	0P42F - 1 = AMPCR	STEP	EXEC		0P42C - 1 =	- 1 =				
					٠												0P4131																						0PC00E 42:							0P42F1					0P420:
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K (P) + 1 INTO R(A); (R(H)) INTO P		K B CONTAINS "A"		K (P) INTO MS WORD OF A2		K (P) INTO US WORD OF A2	(P) + 1 INTO HTR	% (P) + 1 INTO R(A)	K (R(K)) INTO B	% CLEAR PAR FIELD		T PREFARE EAR NEW PAR	CONTRACTOR DAO				K RK TYPE JUMP, LINK REGISTERS					# MAR? CONTAINS ADDRESS OF RCA)	SAVE OLD PAR		E PAD THIN IS UNDO OF AN	HIR CONTAINS (P)		CANADINI SA CANADA SA	THE PART OF THE PA		O = OHE CK IE OHE = O	(BAN) INTO B		X Y INTO P	S CY INTO B	A CLEAR THE PAR		S PREPARE FOR THE NEW PAR	A CREATE THE NEW PAR				REGISTERS	((P) + 2 INTO R(A); (Y) INTO P			A CONTAINS "A"	AUDRESS OF READ IN	K (P) INTO MS WORD OF A2		C (P) INIO LS FORD OF A2	(P) + 2 INTO MIR	K (P) + 2 INIO K(A)		TAINIO B	ואום טאכ	9177	() INTO B
9	: L11	ı,	- 1 = CPCR	A1 L = A2	SAR			= CPCR	M - 1 = CPCR		COMP 16 = SAR		R B = 44	MDCO	1 = 111 CH		-		0 = 0	- []	-	= CPCR	-	COMP 16 = SAR1 2 = 11T	;	M IN	atput - + = Coco	AT AND LIT - AT	15 = 111	A3 FOL P	THEN	 -		- 1 = CPCR			COMP 16 = SAR		A1 OR D = A1 N	0PC00E - 1 = MPCR	_	_	•					- 1 = CPCR	L = A2	16 = SARI 2 = LII	AZ IS = AZ	AZ + LII = MIN			NXMF1ELU - 1 = CFCH 5	COMP A = CAO		ENULIN - 1 = CPCK *
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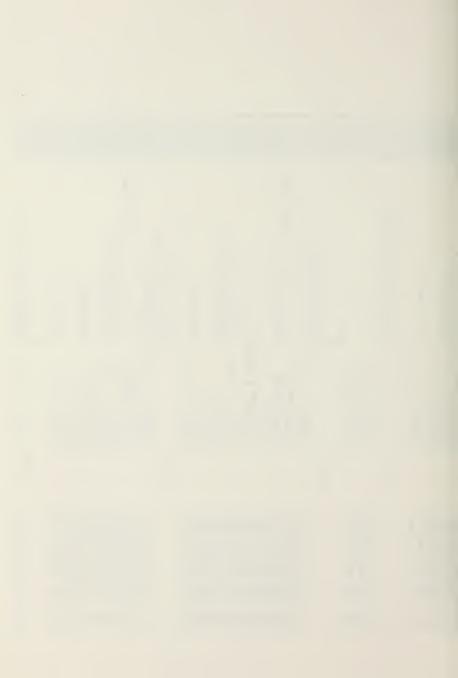
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K CLEAR THE OLD PAR X PREPARE TO RECEIVE NEW PAR X CREATE NEW PAR X JUHP, LINK HEHORY X "F" RETURNED IN AZ	X X RI TYPE 1, LOCAL JUHP, LINK PEHORY S ONLY EXECUTE IF CC = 0 X CHECK THE CC COOF	* PAR INTO AZ (MS WORD) * PAR INTO AZ (LS WORD) * (P) + 1 INTO MIR * PAR INTO UNIV * RESIGNE INSTRUCTION INTO E * O" SIGN BIT IN MS BIT OF R	SET LC1 x 1F *D* NE x *D* HAGNITUDE 1N SAR = BR2xA33 SKIP x (P x (P) + D x (P) + 1 INTO (P)	X (P) + D + 1 INTO B X CLEAF OLD PAK X CREATE NEW PAR X RK TYPE JUHP, LINK HEHORY X (P) + 2 INTO Y1 Y + 1 INTO P X ISOLATE "H" FIELD X IS "H" = 0 ?
A1 R = A1 COMP 16 = SAR A1 L = A1 A1 OF ODE = 1 = MPCR OPCODE = 1 = MPCR A2 + AMPCR = AMPCR SIEP = 1 = AMPCR		0 PCODE - 1 = MPCR 41 L = A2 1 F LC1 COMP 16 = SAR A2 R = A2 A2 L = A2 A3 L = B CSAR B L = B CSAR B D = SAR	R = B = E	18 + 1 = 8 A1 R = A1 A1 L = SAR A1 L = A1 A1 DR E = A1 OPCODE - 1 = MPCR LIT AND 0 = E LIT B E LIT B E DL D
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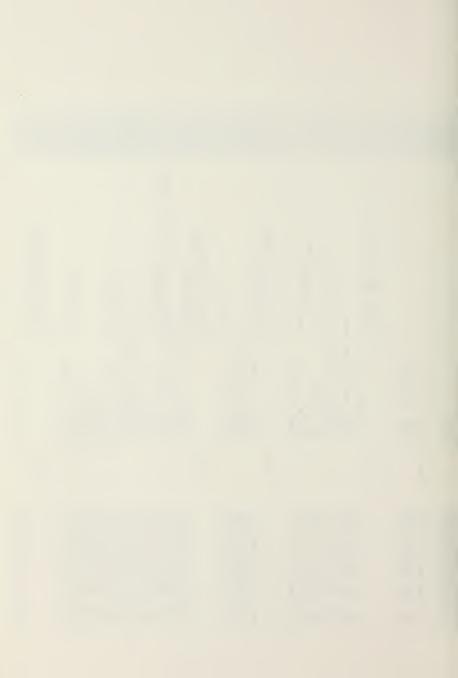
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	N O B			2, A3		`	00000	INS (P)	NTO Y	LS WORE		4 Y 2					W PAR				UMP, LIN	NTO CY)	THE INSTRUCTION				NTO A2		A 2	INS (P)				INTO B			TO ACCEP	W PAR					F* CODE													JMP ZERO	1 C) CH	(K(A))	
	S (R(H)) INTO		INTO 8	Y INTO BEZA	O INI O	1910	CP) TMIN IS LOBO OF AS	HIR CONTAINS (P)	(P) + 2 1NTO	T INTO A3 LS WORD		R CONTAINS V .	CIEAD THE PAC	100			CREATE NIW PAR				RX TYPE J	1 (P) + 2 1		% (Y) IN B			R PUT FAR INTO		(P) INTO A2	MIR CONTAINS		(Y) INTO A3		(7) + 1 1			A1 READY TO ACCEPT NEW PAR	CREATE NEW PAR				JUMP ZERO	RETURNS "F" CODE IN													R RR TYPE JUHP ZERO	* IF (K(A)) = (,, (K(A)) IN	A REICHNS (R(A)) IN	
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Mant and a	CONTENTSRM -	n	H - 1 ::	0 L = 0	6 = SAR	COMP 16 = SARE	= A2	AZ + LIT = HIR	EMULOUT - 1 = CPCR	= A3	SAR	A 1 + 1 = A			2 4 1	= ¥1	A1 UK 6 = A1	OPCODE - 1 = APCR						RXMFIELD - 1	B L = BR2, A3	COMP 8 = SAR	= A2	16 = SAR	= A2	A2 + LIT = HIR	EMULDUT - 1 = CPCR	= A3	SAR	A3 + 1 = B	= A1	SAR	= A1	~	E - 1 =				XFCODE - 1 =	AMPCR =	- 1						"	"	11					B FOI O	
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* RETURNS (R(K)) IN B CLEAF OLF PAR			NEW PAR			F 1 10CAL HIMP FORKE	= 0R 0,	CC DITS IN B				d :: 0			E DY TYPE HIMD 7000	TE (D(A)) O. V. INTO D	A DET COCATA THO	140		SE THE PAR EY 1 AND CALL OPCODE	K "H" FIELD IN A3				S RETURN (R(H)) IN B	a	PAR VALLET IN IN MORD OF F	;			CREATE NEW PAR				A >> = C. CY , CHIO D	# (R(A)) INTO B			ADVANCE THE PAR BY 1 AND CALL OPCODE		ANALYZE THEN "M" FIELD	INIO BRZ	10 8	OLD PAF			CREATE NEW PAR			01 2000	RETURN "F" FIELD IN ISD OF A2
w?			S CRFATE			S RI IYP	1 IF (CC)	# RETURNS				8 (P) +	;		e CV IVE	10 01 1				S ADVANC	S "H" F			41P		V 10.70	8 P 49 V				% CREATE		w 1	200	A 15 CE 6	K (RCA)			A ADVANC		S ANALYZ		S CY INTO	S CLEAR OLD P			S CREATE		e 1	W HIND NOT 7500	S RETURN
HPCR 1 = CPCR	œ			HPCR				= CPCR		SKIF	HPCR	8.0	:				dada = 1	1	SKIP	FCR	A 3			0	1 = CPCF	9595	11.		~			- 1 = MPCR				- 1 = CPCR		SKIP	FCR		= CPCR		CPCK		×			= MPCR			CPCR
OPCODE - 1 = HPCR CONTENTSRM - 1 = A1 R = A1	COMP 16 = SAR	A1 L = A1	A1 0R B = A1	OPCORE - 1 = MPCR				CHECKCC - 1	B E 0 L 0	IF TRUE THEN SKIP	OPCORE - 1 = MPCB	R11 - 1 = HPCR					CONTENTSRA -		IF TRUE THEN SKIP	EUMP - 1 = H	A3 AND LIT = A3	15 = 111	A3 E0L 0	IF TRUE THEN	CONTENTSRH -	TENTON A	A3 + 8 = 8	A1 R = A1	COMP 16 = SAR	A1 L = A1		0PC00E - 1 =				CONTENTSRA -	B E0L 0	IF TRUE THEN SKIP	BUMP - 1 = MFCR	A3 = 9	RXHFIELD - 1	COMP 6 - CAB	FAULTN - 1 = CPCK	A1 R = A1	COHP 16 = SAR	A1 L = A1	=	0PC00E - 1 =			XFCODE - 1 = CPCR
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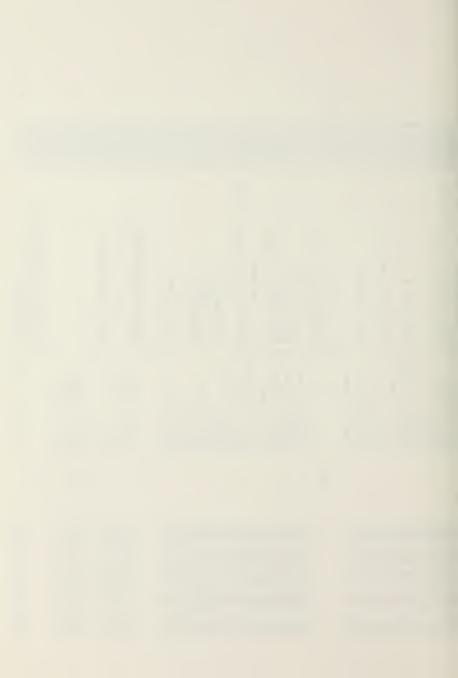
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										RR TYPE	1000	F (RCA)) INTO B		4		RETURN (RCM)) IN			A1 PAR	CREATE				RI TYPE JUMP NOT COUAL	PUT CC BITS IN B	3	Ь		(P) + 0		RK TYPE	IF (K(A)) NE	S (R(A)) INTO		_	VANCE	-			CPCR & CRCHI) IN		PUL Y INTO				CREATE NEW PAR				RX TYPE JUMP NOT ZERO	IF TREAD NE US	
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1						1 1						CONTENTSRA		IF TRUE THEN	DE - 1	CONTENTSEM	A1 R = A1	16 E	A1 L = A1	A1 OR B = A1	DE - 1						IF TRUE THEN STEP	0E -	F11 - 1 =				CONTENISRA	۱ 0	IF TRUE THEN	BUMP - 1 = MPCR	= [1]	A3 E0L 0	RUE TI	CONTENTSRM -		CH - 1		Y .	A1 L = A1	P 0 = 41	DE - 1				4	٥
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S ISOLATE "A"	RCA) INTO H	K (R(A)) INTO B			I ADVARCE THE PAR BY 1 AND CALL OPCODE		ee many	E (Y) IN B					& CREATE NEW PAR					8 GET "F" COOF IN A2													% IF (R(A)) >= 0, (R(M)) INTO P		# SHIFT (R(A)) TO MS WORD			×		A CITAR THE PAG CITE			S SET UP NEW PAR				RI TYPE 1 LOCAL JUHP >=	IK LS FITS	% TEST FOR <		E SKIP		15 (P) + 0 ≈ P	× 1	100 CO	E TE CECAN N= 0. V INTO P			101
B	-	EINPUT - 1 = CPCK		EF ELSE	BUMP - 1 = MPCR		COMP 8 SAR	FAULTN - 1 = CPCK		COMP 12 - CAE	1 4 1 1 4 1 0 AN	AI L = AI	1 × =	OPCODE - 1 = MPCF				XFCODE - 1 = CPCN	AZ + AMPCR = AMPCR	SICE		2		14		1	- 1 -					2		COMP 16 = SAR	TO THE TANK TO SEE THE TOTAL T		CONTENTED A A COCO	1	COMP 16 = SAR	A1 = A1	A1 0R B = A1	OPCORE - 1 = MPCF					111 601 6		IF TRUE THEN STEF ELSE	0PC00E - 1 = MPCK	RII - 1 = MPCR				CONTENTED - 4 - CPCP		
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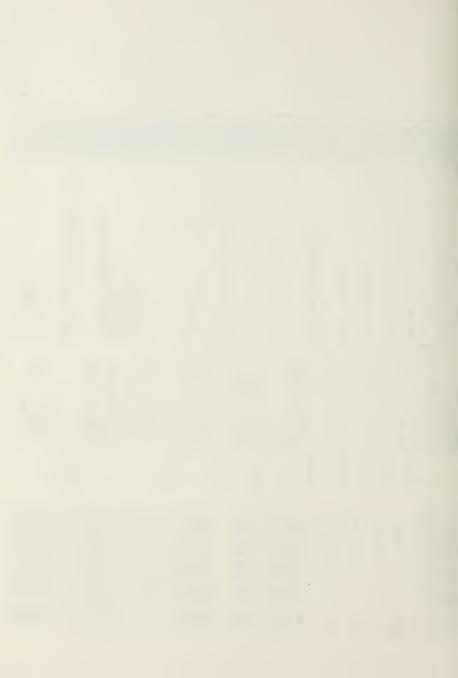
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	CKID	the contract of the contract o		,		16	R (RCH)) INTO 9		# Y 1810 B	o or and and	A PULLAR IN LS HOLD OF B			COLCAD DAD COOM DCU						A RX JUMP POSITIVE	\$ 1F (R(A)) >= 0, (Y) INTO P			C CONTRE SAS TATO D			(K(A)) INIO E	A SHIFT (R(A)) INTO MS WORD OF B		\$ PUT P IN THE ADDER	SKIP	% ADVANCE THE PAR FY 1 AND CALL OPCODE			T PHI Y TAIN BRO	5	e plit (x) tuto o					A CHEALE HEW PAR		**			% RETURNS "F" FIELD IN LSB OF A2				% JUMP TO DESTRED FORMAT TYPE	~	×						 # PR FORMAT THEP REGISTED ACCATIVE	C TE (D(A)) C C. (D(N)) TATO D	A (D(A)) INTO D	
COMP 16 = SAR	THE THEM STED STORE	EL 36	AT AND ATT - AS			THEN 0 =	-		IFFICH - 1 = CPCE	4 6		A1 R = A1	COHP 16 = SAR	41 4 41			Urcule = 1 = Arck					B R = B	4 = SARI 15 = 11T		RECEIACK - 4 - CPCD	4	CINTUL = 1 = CPCR		JHP 16 = SAR		I THEN STEP ELSE	BUMP - 1 = MPCR	A3 = B	PXHFIELD - 1 = CPCK		OVE	d J d J	10 LO	010	COLL TO = SAR		# A1	OPCODE - 1 = MPCR						0P47F - 1 = AMPCF		EXEC			- 1 -	- 1	-	1 1	1			CONTENTS A T = CECE	1
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(R(A))	=======================================	INTO			PAR						8 00 E	CC FOR				0 = P			JUMP	V (INTO	(R(A))		1F (R(THE	INTO		9 9 7 7	A A C O			TA TO				SHIII.							2 2 2	SHIF	100		THE	INC	0 0	. OIN		INTO
<u>-</u> 0	-	S CREMO INTO D			MODIFY PAR 10 JUNE			EI TYPE	1F (CC)		PUT THE CC BITS	CHECK CC FOR 11		SKIP		(P) + (RK TYPE JUMP NEGATIVE	8 1F (R(A)) < 0, (Y) =	K (R(A)) INTO B	SHIFT (R(A)) INTO UHW		CHECK IF (R(A))		ADVANCE THE FAR	(RCH))		PULL PINIO B	FULLAR ALVE			and Jan Tangtanda				NOTTYPE HIMP INSTRUCTION	TE (R(A)) < 0. (Y) = P	CHICL SAS TATA		274 100	DATE TALED	TALL THE CANA	C C V C C C C C C C C C C C C C C C C C	CREAT SHIFTED INTO	CHECK IF (B(A)) <		LOVANCE	DESTONE INSTRUCTION IN C	ANALYTE SMS CATED	PHI Y INTO ARE		S FUT CYD INTO
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= SAR	THENS		= SAR	A 1	¥ .	B 					-	8		E THEN	1 1	= MPCR					SRA - 1		= SAR		U HEN	=	SRH - 1				4 S =		4 11	-	•					1.5	١ ١		• •	-	G 4 S	;	SNEWS	, T		1		= SAR	
B L = B COMP 16	IF MST THEN SKIP		COMP 16 =	A1 L = A1		OPCODE				IF LC1	CHECKCC	LIT FOL	3 = LII	IF FALSE THEN STEP	OPCODE - 1 = MPCR	R11 - 1						B L = B	COMP 16 = SAR		IF MST THEN SKIP	FURP - 1 = MPCR	CONTENTSRH		17 E 1 CH = 1			A 4 1 A 4		DPCODE					E B			DEC TAND	C TANDALT .	0 1 1 0	COMP 46		IF MST THEN SKIP	FUMP - 1 = MPCR	E #	DYMETERS - 4	E I = PR2	COMP 8 = SAR	FAULTN
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A CLEAK THE OLO YAK	S PUT (Y) INTO THE PAR			S NOT IMPLEMENTED			% NOT IMPLEMENTED			8 NOT IMPLEMENTED			* NOTIMPLEMENTED			S 1040 ADDOECC DESTONES	י בפעם אבתופובים אבתופובים											% LAPR: LOAD ACORESS REGS: TYPE RR			E B = (B(M))	,				S B = R(A)		S B = (R(A))	×	R B BIT HASK	% HAR2 = AR		R SEPAKATE AMPCR ASSIGNMENTS				JUNAD ACDRESS REGISTER (INDIRECT)	(Y*) -> AR R				K ((()) (1 × 1 × 1 × 1 × 1
	A1 0R B = A1	0PC00E - 1 = MPCR		0PC00F501	NOTIMP - 1 = MPCR			NOTINP - 1 = MPCR			NOTIMP - 1 = MPCR			NOTINP - 1 = MPCR		OPCODE Sur	XFCOOF - 1 = CPCR	HPCR	P54F - 1		EXEC				- 1	"	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		AS AND LII = 8		4 II	•		LAR: A3 R = D	4 = SAR; 15 = LIT	LIT AND B = B	REGSTACK - 1 = CPCR	FIMPUT - 1 = CPCR	LIT AND B = A2	255 = LIT	A2 + AHPCR = MAR2	PAGEPEG = ANPCR	STEP	1 - 1	0PC00E - 1 = MPCR		0P541:		A3 AND LIT = B		FINDAT - 1 = CFCR	0	0 L = 8K2
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(7+)				A LAMMI LUAD AUDRESS REG. PULLIPLE	ACT PO COTOU) -> AR POCCAR R+U	A MULTIPLE LOADS OFSERVE PAGE	SSES					IAI FIELC		= (R(A))	= PAGE REG NUM.		AR R		B HAS COUNTY ICT SET FOR B 41 MOVE	ALL BEG	ברים מיים ברים שנה שום מיים	EKIP SKIP		COUNT IN UNW OF A3	DRIETN ADDR 18 BB4	Tug ut uggs					Canalarasa asama adula	AUDRESS REGISTERES)											STURE ADDRESS REGISTER (REGISTER)C6941CD0	TYPE RR: (AR) A -> RH				= RA	3(4))	REG NUM.			PAGEREG EAST + REG #	SEPARATE AMPCH ASSIGNMENTS	(AR)		1: 11-10		
X B = C				A LAKIL	X (7)	* MULTIP	A ADORESSES	H H				1 = 3 ×			X A2 = F		R A3 = 1		S A H AS		SAR	. B			K ORIGIN												۳					*		K TYPE A					_	A 2 =				% SEPARA	11 CD	1	ı = /	# HARD =	
FMULIN - 1 = CPCR	H.	LAR - 1 = HPCR						RXHFIELD - 1 = CFCR	H 10	A 3 A 1 B	4 = SARJ 15 = LII	CII AND B = 6	REGSTACK - 1 = CFCR	EINPUI - 1 = CPCK	255 = LII I B = SAR	LIT AND F = A2	A2 + AMPCR = A3	PAGEREG = AMPCR	B R = B1 SFI 1C1	C E01. B			0 + 1 L = 9	A3 OR B = A3, BH1	B I = BR1	COMP A = CAD	May = 1 = CPCR		٠,	,		XCC00C = 4 = 000CC	A2 4 AMPCD - AMPCD		STEP	EXEC			1	1 1 1					. B	4 = SAR1 15 = LIT	LIT AND B = B	REGSTACK - 1 = CFCR	EINPUT - 1 = CPCR	LIT AND B = A2	255 = 1.11	AZ + ANPUR = HARZ	PAGERIG = AMPCR		CINPUT - 1 = CPCE	B = TIN ON F F	ı	7	•
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1	% (AR) -> RM			R TYPE RIS (AR) A -> YM			X I = :AF FIELD	FAR2 = R.	1 (R(A))	* AZ = KE6 #			A PAGEREG EASE + REG II		X B = (AR)		F P = 1M1 FIELD			S [= (R(M)) = Y*			K (AR) -> Y*		CIONE ADEDECE DECICION MILITADIC			A DORESSES		S MIR = Y			K G = :A: FIELD			% A2 HAS PAGE REG #		24 FP III AR R			% A COUNT OF ZERO HEANS ALL REG STORED	21	L = Br SKIP		CRIGIN ACDR IN BRI			DESTINATION ADDR IN LHW UF AS				C NOT THREE PHENTED		\$ NOT IMPLEMENTED		
	OPCODE - 1 = CPCR		0P551r		B (0 1 0	ETABLE - 1 = CPUK	10 10 10 10 10 10 10 10 10 10 10 10 10 1	ZY = JZC	111 = 567	12	TEG = AMPCR		FINPUT - 1 = CPCR	B = MIR	A3 AND LIT = B	1	REGSTACK - 1 = CPCR	1 = CPCR		COMP 8 = SAR	= CPCR		005531				RXMFIELD - 1 = CPCR		8 11 8	4 = SAR1 15 = LII	8	= CPCR		LIT AND B = A2	255 = LITI 8 = SAR		G = AMFCR			11 -	N L11 + 1	1 [= 8	A3 L = BR1	ž		MOUNT AND CA	104E - 1 - CTCR	1 = 111 CH		OPCODE56:	NOTING - 1 - MPCD	0PC00E571	NOTIMP - 1 = MPCR	
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														R RL TYPE LOGIC RIGHT SINGLE SHIFT	I SHIFT (R(A)) RIGHT M (0-3), SET CC,			OF OUR PERSON				SET THE CONDITION BITS	3				I RE TYPE ALG RIGHT SINGLE SHIFT	R (R(A)) RIGHT N (C-3), SICN FILL, SET		S (RCA)) INTO B									X A2 = 000C/COCO OR 1111/CCOC		% B = 1111/(R(A)) OR C000/(R(A))		T PERFORM ALG RIGHT SINGLE SHIFT						A SEL THE CONDITION BILS		*		8 (R(A),R(A+1)) M (3-3) PLACES, 7ERO FIL	AND CET CC	22 127 254 8				N OBIAIN "A" FIFLD					K (R(A)) INIO 6
900	AFLUNE - 1		OP60F - 1 = AMPCR	STEP	EXEC					H ~	-			•	-	CONTENICOA - 4 - CPCO C		AND LIT = A3	15 = LIT	A3 = SAR	B R = MIR. B	I CPCR	0000	E001701 - 1 = CFCR	OFCODE - 1 × NFCK			-	IF LC1	CONTENTSRA - 1 = CPCR	•	2 1 2	,	11		IF MSI IMEN BILL = AZ	AND LIT = A3	COMP 16 = SA	12		A2 OR B = B	A3 = SAR			0 40 - 74 0	10 10 10 10 10 10 10 10 10 10 10 10 10 1	ALE CO H A H	001FUI - 1 = CFCK	- 1 = CPCK	0PC00E - 1 = MPCR						II AND B = AZ	15 = LIT# 4 = SAK	B R = B	LII AND 8 = P	EFCR		CITAR L CONT	= SAK	EINPUT - 1 = CPCR
6	OF COULSO						* 50 7 00							0P600s													0P6011																									0P602:												
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1	1 £ 6 B	156C	1560	156E	15 6F		0000	12/0	1571	1572	4573	1010					1: / 4	1575	1576	1577	4 5 7 9	4570	1217	1: / /	1 4 78				1576	45.70	2 1	15/6	1/21	1580	1581	1582	1583	15.84	1585	1: 96	15.87	1588	15.00	100	100	1 00	15 80	1 . 80	15 BE	158F						1590	1591	1592	1503	1594	1505	1272	1596	1597



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1 = LIT		16	11 R R R R R R R R R							
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		255 000 000 000 000 000 000 000 000 000	0010 0000 0000 0000 0000 0000 0000 000		SHIFT ION BIT	* NEW (R(A+1)) * WRIE NEW R(A+1) * REFRENCE OR 1 * R(A) * (R(A))		TEHP CRC)		PERFORM SHIFT B = 1111/00CC OR B SET THE CONDITION B (R(A+1)) SHIFTED IN REFERNCE 9R1
		25.50 00.00	4809 2 25 5 0010 0040 0040 0040 0040 0040 0040 0		SAR = A3.61 SET LC1 :A - 1 = CPCR	16 = SAR 116 = SAR 11		4 5	N SEI LC1 SAR 7 1 = L1 R = HAR2 = CPCR	EN B111 = B A3.99. SET LC 1 = CPCR SAR R 1 = CPCR
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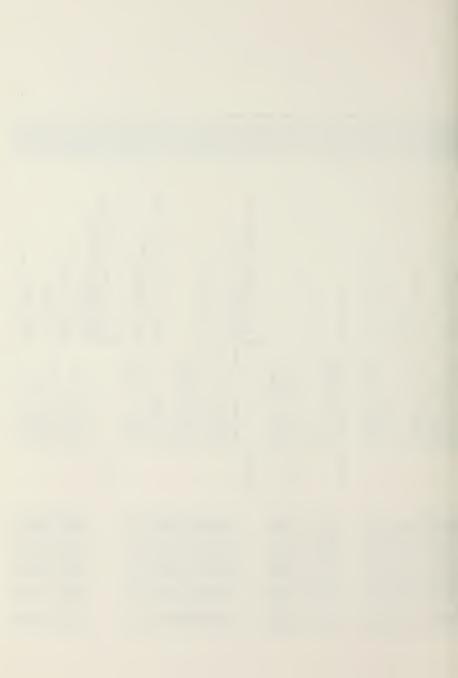
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																		-		80 5	SET CC AND SET OVERFLOW (11																									F	(R(A)) SHIFTED H (0-3) PLACES,												TATIO	-				
																			RE TIPE ALG LIFT SINGLE SHIFT	, 7E	0.40																					S				TYPE RL CIRCULAR LEFT SHIFT) PL												4 COMPLEMENT OF SHIEL ANDHMY					
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		(2)																		3	ET 0	10 A2						ند			SHI					-	1 .			S	(())	ITION				ULAR	FO H				FIFI		Œ				1000			5				
		MALIE NEW CKCAJ				٧5												:	٠,٠	- 60	NND S	"H" FIELD INTO			* *						PERFORM LEFT SHIF					A CONTRACTOR LINE ALCOHOL	1			LEFT SHIFTED (R(A))	WRITE NEW (RCA))	SET THE CONDITION BIT				CIRC	HIFT	V 7			. Y .		NTO				- (0(4))/(0(4))		N L	11011	PERFORM SHIEL	,		
		ž				2												1	1	2	200	FIEL			TCOLATE SAS			CREAD INTO			ORM					7	2			SH	TE NE	T HE				R.	000	"H" INTO A?			ATE		(R(A)) INTO				, 00	G C I Z I S N S	- 01		HOU			
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	SAR SAR	- 10.1.00	UPCODE			XFCO		11011	200	د		01000	0 6 6 1 1	0P612	0P613							LII AND B	= -	B R = B	A AMA TI	DECCTACK - 4	TO SO I TO MAN TO SO I		NO 1 A 2 A 2	•	8 F = B	B R =	16 = SAR	CA TON	NO	DOC - F - LIGHT	1 1 1 1 1	_ ;	COMP 16 = SAR	PR = MIR, B	EDUTPUT - 1 = CPCR	ETCCA - 1	OPC ODE					LIT AND P	15 = LITI	PR = B	LIT AND B =	REGSTACK	EINPUT - 1	B = A3	A 3 L =		A 4 00 B =				, ,		COMP 16 =	
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WRITE DUT NEW (G(A)) SET THE CONDITION DITS	RL IYPE ALG LEFT DOUELE (HIFT (RRA), MR(A+)), H (G-3)	O FILLS SET CC. AND SET OVERFLOW		ISOLATE "A" FIELC	TEMP STORAGE OF R(A)		(R(A)) INTO P			(R(A+1)) INTO B A3 =(R(A))/(R(A+1))					SEL IME OVERFLOW BIT		ET THE CONDITION BITS			PEFFERENCE PRI				OUTPUT (R(A))		_	COCANOCARANO H COLIN AND CET CO					TEMP STORAGE		(R(A)) INTO B			A+1) INIC E	= (K(A))/(K(A))
	R RL			X 150	TEH		£ (R)			X X					2 F		o																				ž	2
A3 R = MIR, 6 E0UTPUT - 1 = CPCR SETCCA - 1 = CPCR OPCODE - 1 = MPCR		8 8 8		-	= CPCR		FINPUT - 1 = CPCK	COMP 16 = SAR ; 1 = LIT		A3 08 B = A3		A2 + 1 = SAR	NO 1 B 10N	IF NOT ABT THEN SET LC1	A2 + 1 = SAR	SET LC1	At I = B	COMP 16 = SAR		ASR SR	= MAR2	8 = CAR	16 = SAR	EDUTPUT - 1 = CPCR S	OPCODE - 1 = MPCR		et bi		15 = LIT 1 4 = SAR	B X II B	= CPCR		6	EINPUT - 1 = CPCR 8	COMP 16 = SAR; 1 = LIT		AT OR B = AT	
	016121																										01-613:											
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4 CIRCULAR SHIFT 8 SCT THE CONDITION BITS		# OUIDUI SHIFITO (R(A))	TYPE RL SUBTPACT, (6 FT (c, CARRY AND OV RR(A)) INTO E	2 0	* (R(A))-H INTO R(A) * TYPE RL LITEPAL SUBTRACT DOUBLE ** TR(A), PR(A+1) * SET (C, CARTA AND OV BITE * SHIFT A" 10 LS 4 BITS * ISOLATE "A" FIELD * TEMP STORAGE ** (R(A)) INTO HS NORD OF A?
A2 + 1 = SAR A3 C = A3.01 SET LC1 N SETCCA - 1 = CPCR	16 = SAR HIR SAR PUI - 1 = CPCR R = HAR2 SAR = HIR	U1 - 1 = CPCH E - 1 = MPCR ODE - 1 = CFCR AMPCR = AMPCR - 1 = AMPCR	CONTENTSRA - 1 = CPCR OP622 - 1 = NPCR OP623 - 1 = CPCR	L = A5 A0 15 = L1 3 A00 L11 = B 3 A00 L11 = B 4 D = HIR1 SCI (C2 7 D = HIR1 SCI (C2 7 T A0 Y HEN EFI L1 4 REVOY - 1 = CPCR HI C C C C C C C C C C C C C C C C C C C	0P621: 0P601: 1
COCO OCOC 80F0 E001 980 COF0 0000 000 000	00000			2000 0000 0000 0000 0000 0000 0000 000	202 0000 0000 0000 0000 0000 0000 0000
1632 4809 CC 1633 4909 EC 1634 2000 OC	4800 4800 4800 4800 4800 4800 4800 4800		1FFC 2000 2010 2010 228C		4809 4809 4809 4809 5310 74809 6000 7510 7610 7610 7610 7610 7610 7610 7610 76



OZSTACOO D				07371000 0	07322660 0		0000			0 30392570		_	_	C733CC00 D	07331C0C n		07111000			0.0000000000000000000000000000000000000					C734CC00 D	C7341C00 P	07342C00 C	07343600 0	07344500 6			20.20	07347500			0.7355.00		0.0025200			0 0035560	0735560	0115.000.0		0 00329270		C7364C0C D	07365000	07366000 0	07367C00 B		_	07370000	_	_	07373660 0	0737460C D	_	0/3/6/00 0	13/100 0
	•		(KLA)))																							(R(A))+E -> R(A)	AND 0V 9115	3				a	1							u	,			TYPE RI LITERAL AND DOUBLE	SET CC. CARRY, AND DV BITS									WORD OF A?						
X R(A+1)	S CRCA+133 INTO B	4 42 = (B(4)) ((B(4)))	•												K NEW (R(A+1))		A PFF 5R1			1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1				pt (*	TYPE RL LITES	۳	A CRCADO INTO E		111	S ISOLATE "N" FIFID									THE COMPITION DIT	C COCANAM INTO OCAN				S SET CC. CARRI			K "H" INTO HIR		R(A)			S (RCA)) INTO 6	(RCA)) IPTO			8 (R(A+1)) INTO B			
LIT OR BHAR = MARZ	FINPUT - 1 = CPCR	42 00 B = 42, BH?	1110 174 - 0 10 34	AZ - 9 = MIRI SEI LCZ	IF ADV THEN SET LC1	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR	BALL SET LET	0.000 - + - 4.0000	DATE OF THE COLUMN		0 L = AC	COMP 16 E SAR	E 11 H	A2 R = MIR	FOUTPUT - 1 = CPCR	ASR	BHAR R = MAR2		2 2 2	•	COULD - 1 = CFCR	UPCODE - 1 = HPCK					CONTENTSRA - 1 = CPCR	B L = A2	COMP 16 = SAR1 15 = L	A3 AND LIT = B	8 1 1 8	A2 + 8 = MIR	IF ADV THEN SET 1.C1	CADDY - 4 - CDCD	Cuttory Coco	4	B R = MIR.B	16 = SAR	SFICCA = 4 = CPCP	FORTPILL 4 = CPCR	OPCORE - 1 = MPC8				B R = 8	4 = SAR1 15 = LIT	A3 AND LIT = MIR	LIT AND B = R	REGSTACK - 1 = CPCR	BMAR L = BR1	COMP 8 = SAR	EINPUT - 1 = CPCR		**	LIT OR BFAR = MAK2	A2 A2 A - A2 A41	AC UK U = AZ# UFI	IF ADV THEN SET 1C1	
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								S NEW CRCA+133		# REF CRI			K NEW (R(A))				S STS INTO A											SET C.	L ISOLATE "M"			# ISOLATE "A"		& WRITE "H" INTO R(A)				S RI TYPE LITERAL COMPARE. (REALLSH		I "H" INTO HIR			A CREAT TRIDE	CREALL INTO HIS WORD OF AZ		S SET THE CONDITION BITS						
	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR	BMI SET LC1	SEICCA - 1 = CPCK		CAN = 1 6		H H IR	PUI - 1 = CPCR		= HAR2	8 = SAR		FOUTPUT - 1 = CPCR	OFCODE - 1 = OFCR			A2 + AMPCR = AMPCR	0P63F - 1 = AMPCR	STEP	FXEC	00000		0P631 - 1 = DPCR	1		0P630:			,	S = 0 × V		REGSTACK - 1 = CPCR	æ	SELOU - 1 = CPCR	urcout - 1 = arch		0P631:		3 = MIR	15 = LIT	900	* C.C.*	COHD 42 = 240		1 = CPCR		IF ADV THEN SET LC1	CARRY - 1 = CPCR	CHECKOV - 1 = CPCR	0PC00E - 1 = MPCK	K W
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1	1695	1696	1691	1698	1699	1698	1691	1690	169E	169F	16 40	16A1	16 A2	16A3	10 44		16A5	16 A 6	16 A 7	16 A B	16 A 9	4 6 4 4	4 4 4 5 4 5 4 5	16 AC	16 AD				16 AE	1680	1681	1692	1693	1684	1693	1000				1697	1688	1689	4 4 8 8 8	1 / BC	1680	16BE	16 BF	1600	1601	1602	1603	



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), SET CC																											REMAINDER																										
TYPE BILLIEGAL MAN THE X	R(A+1) X M = (R(A),R(A+1)),			# ISOLATE "A"	TEMP STORAGE	,	R(A+1)	R(A+1) INTO PAR?	(R(A+1)) INTO B	"H" INTO A2		(R(A+1)) X N INTO A3	A PRODUCT INTO B. MIR	SET THE CONDITION BITS			R(A+1))		REF FR1	RCAD		N. A. J.					TYPE RL LITERAL OIVIDE	(R(A),R(A+1))/M = R(A+1), RENAINDER	NTO RCAD, SET CC AND DV	ISOLATE "H"		LEFT JUSTIFY DIVISOR		ISOLATE "A"	R(A) INTO HAR2	STORE R(4)		(RCA)) INTO F		0,440	E F(A+1) INIO HARD	S (RCA+1) INTO B	LC1 8 A2 = (R(A))/(R(A+1))	K (RCA),RCA+1))/N	REF GR1	R(A)		REMAINDER		COUNTIENT INTO By MIR	SET THE COMOTTION CODE	R(A+1) INTO BAR2	QUOTIENT INTO RCA+13	cer ov 817
	- W			×				* R		×		×		SE			×			×					×	pr	X I Y	# C H	-			×			S FC			×		9		S CR	101		# RE	R. R.C		S RE) i	200	2 2 2	00	A CE
			4 = SAR; 15 = L11	LII AND B * B	PHAR L = BR1	COMP 8 = SAR	-	REGSTACK - 1 = CFCR	EINPUT - 1 = CPCR	A3 AND LIT = A2	15 = LIT	MULT - 1 = CPCR	A3 = B, MIR	SEICCA - 1 = CPCR	A3 L = B	COMP 16 = SAR	H H H H	EDUTPUT - 1 = CPCR	ASK	HARR R = MARZ	C 2 1 0 0 2 4 4	1		0PC00E - 1 = MPCR		•					15 = LII7 CUNP 18 = 5	# # B - B	2 W 0 W 17	LIT AND 0 = E			COMP 8 = SAR	FINPUT - 1 = CPCR	COMP 45 = 540	BAAD + 4 B	REGSIACK - 1 = CPCR	FINPUT - 1 = CPCR	A2 OR B = A2, BMI; SET	01V - 1 = CPCR	ASR	RHAR R = MAR2	8 = SAR	A2 = HIR	EDUTPUT - 1 = CPCR	AS = B, MIR	SEICCA - 1 = CPCR	REGSTACK - 1 = CFCR	· =	
0P6321		-																									0P6331																											
		0 F C	0080	0 10 3		0030	COFC	0900	0900	0.100	0.00	0903	0.010	0900	0 0 E 0	0000	0 100	0900	2 OF 0	0.00	0100	0.00	0.06 C	0 0 0 0						0010	0100	0 100	0000	C 0 F 0	2903	0 0 t 0	0030	3900	0.00	COFC	0900	0.06 C	0 0 E O	0 9 0 0	2 O F O	0 O E O	0 0 1 0	00FC	0900	0010	0000	0900	3903	390)
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			4 1 1 2 1 A 1 A 1 A 1 A 1 A 1 A 1 A 1 A 1					a DINI I							CPCR & (R(A)) INTO			SKIP		I ISOLATE MS B'				K FERFCRM ADDITION								A SET THE CONDITION BITS		GET LS BYTE (*							SET CC, CARRY		X Y INTO B			K (Y) INTO B			
	Uress - 1 = HPCR					SET 102	DVHFIELD = 4 = CECD	0	COMP 4 = 540	COLL G - SAR	ETULIN - 1 = CPCh	6 L = MIR	COMP 16 = SAR		1	B L = A2, BHI	COMP 16 = SAR	IF LC2 THEN STEP ELSE SKIP	LS653 - 1 = MPCR		24 = SAR	8 [= 8		A2 + B = HIR	IF ACV THEN SET LC1	=	CHECKOV - 1 = CPCR	BHI	B R = B, MIR	16 = SAR	œ	SETCCA - 1 = CPCR	OPCODE - 1 = MPCR	UL = B, CSAR	CUMP 8 = SAK	C K = 8 C K S 3 = 4 = HP C 9			OPCODERS XFCODE - 1 = CPCB		0P66F - 1 = AMPCR		FXEC		- 1	- 1 =		= PPCR	-	-			- 1 = CFCR	9 L = BR2		ENULIN - 1 = CPCR 1	1 = 11K	A3 11 B 12 C	2
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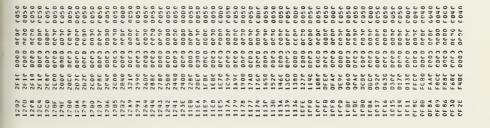
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SKIP K GET LS BYTF OF (Y) K HS (Y) BYTE INTO HSW OF (1, A3	R SET THE LONDITION BITS	TYPE RX GVTE COMPARE AND INDEX BY 1 \$\$ (RRA) > 1 INTO RCH) \$\$ SET CC_CARRY_AND OV BIT \$\$ RVTF OPERATION FLAG FOR RXHEIELD \$\$ Y INTO B	A (R(A)) INTO HS WORD OF AS SKIP A HS (Y) EYTE INTO HS WORL OF B
CONTENTSRA - 1 = CPCR L = A2 DNI CORP 16 = SAR L L CZ TMEN STEP ELSE LS663 - 1 = KPCR R = P R = SAR R L = BA A3 A2 - 0 = HR3 SET LC2		NUTINF - 1 = NPCK NUTINF - 1 = NPCK NUTINF - 1 = NPCR NPCS - 1 = NPCS NPCS - 1	558A - 1 = CFCR 5 = 58H 5 = 58H 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 = 1 =
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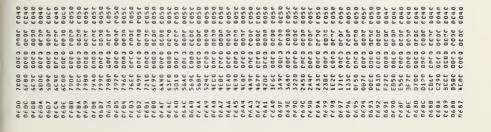
















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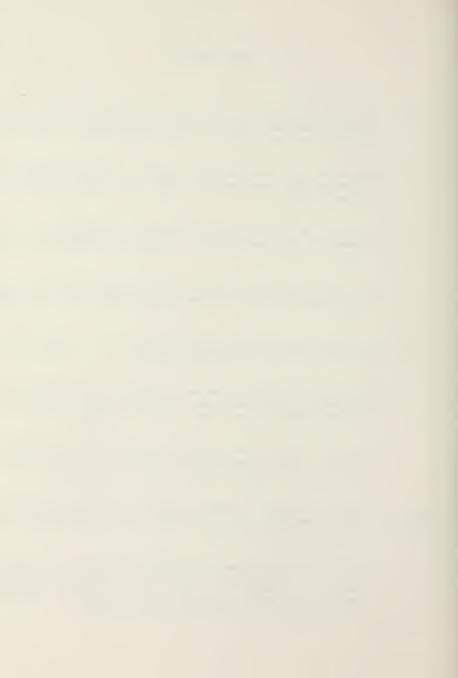
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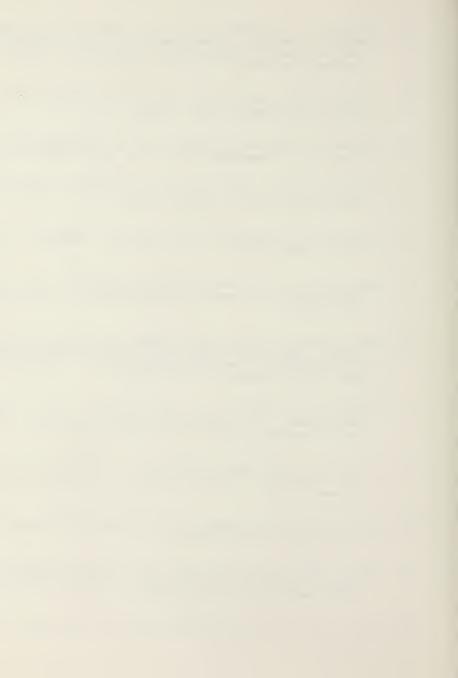


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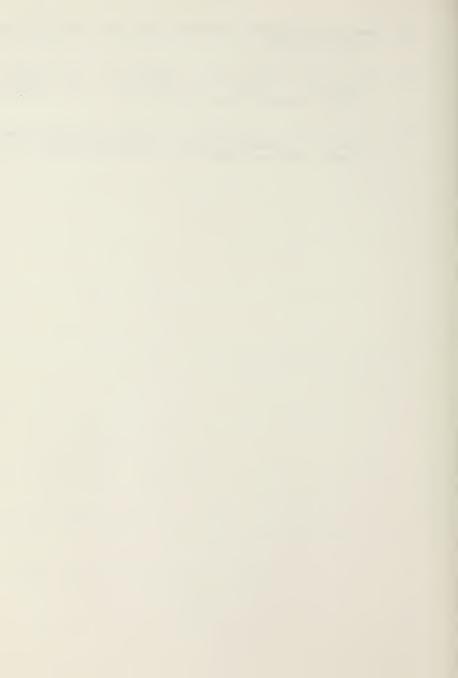
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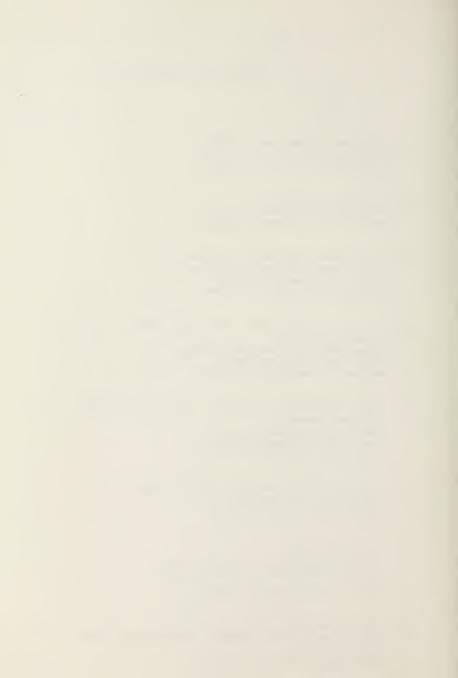


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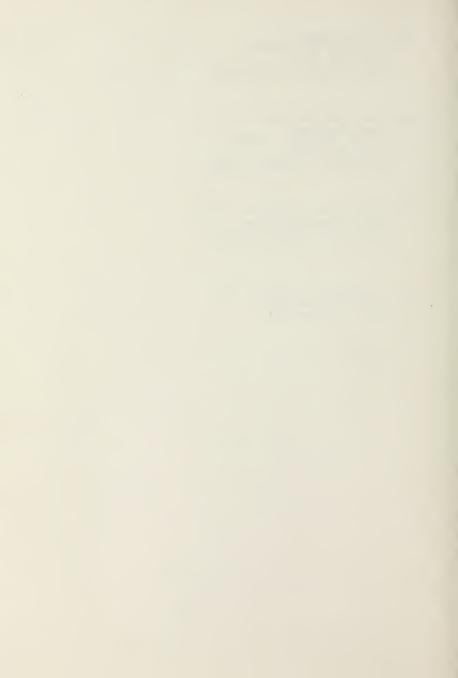
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